CASCADE TOPOLOGIES FOR THE ASYMMETRIC MULTILEVEL INVERTER BY NEW MODULE TO ACHIEVE MAXIMUM NUMBER OF LEVELS

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ABSTRACT: Multilevel inverters have been introduced as useful devices to connect between DC-AC systems. Their high quality output and costs benefit a wide range of applications. Asymmetric multilevel inverters are a type of multilevel inverter with an unequal DC link to create more voltage levels through fewer components. This paper presents new topologies of cascade multilevel inverters by a new module with reduced components. The base module produces 13 levels with two types of unequal DC sources and 10 switches. Modular can be used to produce more and higher voltages levels. The designing of proposed multilevel inverter makes some preferable index with better quality than similar modular multilevel inverters, such as less semiconductors and DC sources, low switching frequency, creating of negative levels without any additional circuit, and module in cascade connections. Also, two cascade topologies are presented in the modular connections of the proposed module to achieve high and significant number of levels. Nearest level control (NLC) method as a switching technique is used in step changing levels for topologies to get more quality and lower harmonics. The presented module and cascade topologies are simulated by MATLAB/Simulink and are implemented by the experimental prototype in laboratory to validate the performance of proposed topologies in which simulated and experimental results show a good performance. THD% (Total Harmonic Distortion) of the module and cascade topology in experimental results calculated 4.94% and 2.05% respectively that satisfy harmonics standard (IEEE519).

ABSTRAK: Inverter pelbagai peringkat telah diperkenalkan sebagai peranti berguna untuk menyambung antara DC-AC sistem. Sistem ini memberi output dan faedah kos berkualiti tinggi dan mempunyai pelbagai aplikasi. Inverter pelbagai peringkat asimetrik adalah sejenis inverter pelbagai peringkat dengan pautan DC yang tidak sama rata untuk mewujudkan lebih banyak paras voltan menerusi lebih sedikit komponen. Kertas kerja ini membentangkan topologi baru inverter pelbagai peringkat lata melalui modul baru dengan komponen yang dikurangkan. Modul asas mengeluarkan 13 peringkat dari dua jenis sumber DC tidak sama rata dan 10 suis. Modular boleh digunakan untuk mengeluarkan tahap voltan yang lebih banyak dan lebih tinggi. Mereka bentuk inverter pelbagai peringkat yang dicadangkan menghasilkan beberapa indeks dengan kualiti yang lebih baik daripada inverter modular pelbagai peringkat yang serupa, saperti sumber semikonduktor dan DC yang lebih rendah, frekuensi pensuisan yang rendah, kejadian tahap negatif tanpa sebarang litar tambahan, dan modul dalam sambungan lata. Juga, dua topologi lata ini dibentangkan dalam sambungan modular daripada modul yang dicadangkan untuk mencapai jumlah yang tinggi dan tahap yang ketara. Kaedah Tahap Kawalan Terdekat (NLC) sebagai teknik pensuisan digunakan dalam tahap langkah

berubah bagi topologi untuk mendapatkan harmonik yang lebih berkualiti dan lebih rendah. Topologi modul dan lata yang dibentangkan disimulasikan oleh MATLAB/Simulink dan telah dijalankan oleh eksperimen prototaip dalam makmal bagi mengesahkan prestasi topologi yang dicadangkan di mana hasil simulasi dan eksperimen menunjukkan prestasi yang baik. THD% daripada topologi modul dan lata dalam hasil eksperimen adalah 4.94% dan 2.05% masing-masing yang memenuhi harmonik standard (IEEE 519).

KEYWORDS: *asymmetric; component; multilevel inverter; power electronics; NLC*

1. INTRODUCTION

Energy is a key concern to the world. In the 1970s, during the energy crisis, renewable energy and other supplies of DC power became possible alternative sources of energy to replace carbon-based fuels. Recently, solar and wind sources have seen increased deployment because of their accessibility and non-polluting characteristics. Power electronics and multilevel converters play a crucial role in improving these typically DC systems. Multilevel converters have been one of the main subjects for DC systems research in the past decades because of their interesting features such as high quality output voltage, operation at high voltage/power levels, low stress on switches as switching frequency decreases, and rated voltage. Also, multilevel converters have a very wide range of applications [1-6]: HVDC systems, photovoltaic and wind plants, active power filters, and electrical machine drives. Multilevel converters are different arrangements of power electronic switches with DC links to create n-level waveforms on the output.

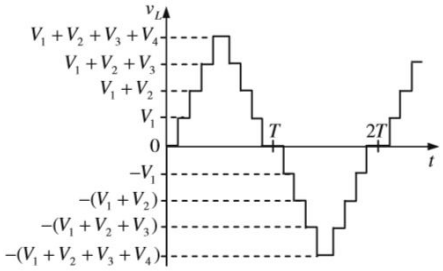


Fig. 1: N-levels waveform on multilevel inverter output (9-levels).

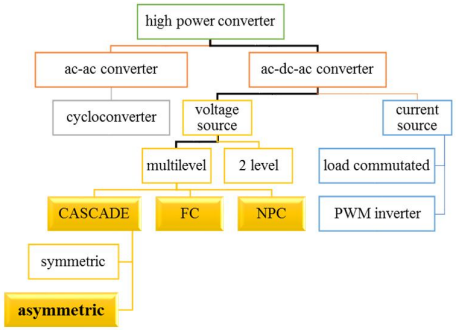


Fig. 2: Inverters categories.

Figure 1 shows a sample waveform of multilevel output with 9 levels. Generally, multilevel converters are divided into three types [7]: NPC (Diode Clamped), FC (Flying

Capacitor), and CASCADE (Cascade H-Bridge). In 1981, the first multilevel converter introduced was of the NPC type. It could be used for medium voltage levels [8]. By the early 1990s, FC was presented [9], and in 1996, CHB was reintroduced [10]. Figure 2 shows the various categories of converters. In Fig. 2, there are two types in CHB multilevel, specifically: symmetric (with equal DC link), and asymmetric (with non-equal DC link).

The design of asymmetric multilevel inverters considers many parameters: the number of levels, semiconductors and DC links, the amplitude of THD (Total Harmonic Distortion), the maximum voltage level, the creation of positive and negative levels, modular ability, and switch stress. Researchers have presented different types of modular multilevel converter. In [11], two switches and one source create each level. These levels are added together to reach (n/2) levels. In the end, an auxiliary circuit (H-bridge) is used to create negative levels and n-levels are added. H-bridge switches tolerate higher voltage than other switches. In [12], the H-bridge is divided into sub-modules with two capacitors added for each DC source to find more levels without requiring more semiconductor devices. Researchers have tried to reach more levels with fewer components. Modules are designed based on optimal use of DC sources by reduced switches [13-15]. In addition, a modular ability is considered to find higher voltage in topologies [16, 17].

There are several parameters to design ideal multilevel inverters for various applications. Some parameters are more important for some applications. For example, there is a high stress switch circuit on the end of H-bridges for high voltage applications. Redesigning modules to divide the H-bridge into sub-modules leads to increases in the number of semiconductors and thus leads to higher construction cost. Also, the total standing voltage (TSV) is raised on the module. Using the maximum capacity for the DC link can be achieved by suitable arrangement of the switches in a suitable topology. This arrangement improves economic cost of implementation, switching frequency, TSV, the number of levels, and THD.

This paper presents a new asymmetric multilevel module with new cascade connection topologies. The module can be used as two cascade method connections and it does not need any additional circuit to create negative levels. Also, it makes 25 levels in the first method and 169 levels in the second method using only two modules. Section 2 illustrates the proposed multilevel inverters including module description, switching patterns, and cascade connection in each of the two methods. Nearest level control (NLC) method is introduced for switching modulation in section 3. Simulation and experimental results of the proposed topologies are shown in sections 4 and 5.

2. PROPOSED MODULE

The proposed topology is illustrated in two parts: module configuration and cascade connection topologies.

2.1 Module Configuration

This subsection introduces a new asymmetric modular multilevel inverter featuring new component arrangements including 10 switches, 10 diodes, and 4 DC supplies with different voltage outputs (two $2V_{DC}$, two $1V_{DC}$). The arrangement of these components is very smart to produce 13 levels (6 positive levels, 6 negative levels, and a zero level) without any additional circuitry to create negative levels. Additionally, negative levels are inherent to the model and it does not need an H-bridge converter. Figure 3 depicts the proposed module.

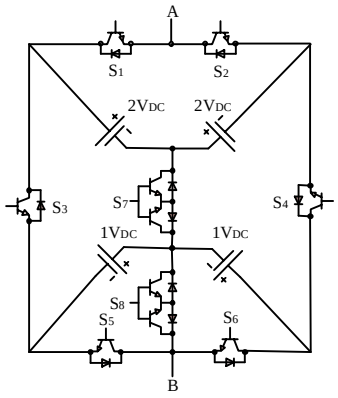


Fig. 3: Proposed multilevel inverter.

Of 10 switches, 4 switches work as two pair (S_7, S_8), which means the module has 6 unidirectional switches and 2 pairs of bidirectional switches. It helps to reduce switch drivers down to 8 drivers. 4 DC supplies are different amplitude to create different levels of output. Also, equations for the number of components are written as follows:

$$N_{levels}=12n+1 \quad (1)$$

$$N_{switches}=10n \quad (2)$$

$$N_{diodes}=10n \quad (3)$$

$$N_{Drivers}=8n \quad (4)$$

$$N_{DC\ links}=4n \quad (5)$$

$$Total\ Standing\ Voltages\ (TSV)=20n \times V_{DC} \quad (6)$$

where N and n are the number of levels and module units, respectively. Eqs. 2 to 6 can be rewritten as Eqs.7 to 11 based on number of levels (N_L):

$$N_{switches}=5(N_L-1)/6 \quad (7)$$

$$N_{diodes}=5(N_L-1)/6 \quad (8)$$

$$N_{Drivers}=4(N_L-1)/6 \quad (9)$$

$$N_{DC\ links}=(N_L-1)/3 \quad (10)$$

$$Total\ Standing\ Voltages\ (TSV)= 10(N_L-1)/6 \quad (11)$$

Table 1 describes the switching pattern and demonstrates that positive and negative levels have symmetrical paths to each other. S_1 and S_4 belong to positive levels and S_2 and S_3 belong to negative levels. Also (S_1, S_2) and (S_3, S_4) cannot be on at the same time.

Three switches are on with some DC sources for each level pattern. Switches S_1, S_6, and S_7 and the upper left side and the lower right side in series from DC sources are used for $+1V_{DC}$. Switches S_1, S_7, and S_8 with the upper left side of DC sources create $+2V_{DC}$. Adding the upper left side and the lower left side DC sources switches S_1, S_5 and S_7 make $+3V_{DC}$. Two upper side of DC sources and switches S_1, S_4 and S_6 generate $+4V_{DC}$. Two upper sides and the lower right side of DC sources and switches S_1, S_4 and S_8 are considered for $+5V_{DC}$. Finally, all DC sources by switches S_1, S_4 and S_5 are used to achieve $+6V_{DC}$. Similarly, the negative levels are available as symmetrically.

The module is designed for switches with low switching frequency. Table 2 illustrates that the switching frequency of each switch per cycle is low. The output voltage waveform has 24 steps for each sinusoidal cycle. If system frequency is assumed to be 50 Hz, there are four switches (S_1, S_2, S_3 and S_4) with a 50 Hz in sinusoidal waveform and the maximum switching frequency is 400 Hz for S_8. This guarantees less switching losses and longer life.

Table 1: Switching table of the proposed module

	Levels	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	the upper left side DC source ($\pm 2V_{DC}$)	the upper right side DC source ($\pm 2V_{DC}$)	the lower left side DC source ($\pm 1V_{DC}$)	the lower right side DC source ($\pm 1V_{DC}$)
Positive Level	$1V_{DC}$	1	0	0	0	0	1	1	0	√			√
	$2V_{DC}$	1	0	0	0	0	0	1	1	√			
	$3V_{DC}$	1	0	0	0	1	0	1	0	√		√	
	$4V_{DC}$	1	0	0	1	0	1	0	0	√	√		
	$5V_{DC}$	1	0	0	1	0	0	0	1	√	√		√
	$6V_{DC}$	1	0	0	1	1	0	0	0	√	√	√	√
Negative level	$-1V_{DC}$	0	1	0	0	1	0	1	0		√	√	
	$-2V_{DC}$	0	1	0	0	0	0	1	1		√		
	$-3V_{DC}$	0	1	0	0	0	1	1	0		√		√
	$-4V_{DC}$	0	1	1	0	1	0	0	0	√	√		
	$-5V_{DC}$	0	1	1	0	0	0	0	1	√	√	√	
	$-6V_{DC}$	0	1	1	0	0	1	0	0	√	√	√	√

Table 2: Switching for each cycle and 50 Hz sinusoidal waveform

Switch Number	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
Number of turning on for each switch in one cycle (13 level)	1	1	1	1	7	7	4	8
Frequency of each switch in 50Hz sinusoidal waveform	50	50	50	50	350	350	200	400

Table 3: Comparison some modular multilevel inverter topology for 13 levels

(For 13 levels)	NPC	FC	CHB	CSMLI [14]	Proposed module
Switches num.	24	24	24	14	10
Diodes num. (+diode clamped)	24+20	24	24	14	10
DC links num.	6	6	6	6	4
Drivers	24	24	24	14	8
TSV (x V_{DC})	24	24	24	24	20
Modular able	complicate	complicate	simple	simple	simple

Some famous topologies are compared with the proposed module in Table 3 to evaluate of number of components. Table 3 illustrates the number of components for 13 levels specifically in NPC, FC, CHB and CSMLI. Table 3 declares that the proposed module has the lowest number components of all topologies. The last column describes

how at least 4 switches, 4 diodes, 2 DC links, and 6 drivers are used in the proposed module fewer than other columns. Also TSV is reduced down to $20V_{DC}$.

2.2 Cascade Connections

The modularity of the cascade connections is another feature of the proposed inverter enabling the creation of more levels and the use of alternative switching paths. Two cascade topologies are considered for the cascade connection to achieve greater performance. In the first cascade topology, each module (unit) has two $1V_{DC}$ and two $2V_{DC}$ DC links. Units are joined in series to obtain the output voltage (see Fig. 4). In this topology, multiple units can create the total output voltage. In other words, for two units, 6 levels are added on positive levels and 6 levels are added on negative levels (adding of 12 levels, totally). Also, there are more switching state choices for each level which causes a high reliability. For example, there are 10 switching paths to produce total output voltage for $V_{out}=3V_{DC}$ Where Vj is output voltage of unit j:$(3V_1+0V_2)$, $(2V_1+1V_2)$, $(1V_1+2V_2)$, $(0V_1+3V_2)$, $(-1V_1+4V_2)$,$(-2V_1+5V_2)$, $(-3V_1+6V_2)$, $(4V_1-1V_2)$, $(5V_1-2V_2)$ and $(6V_1-3V_2)$.

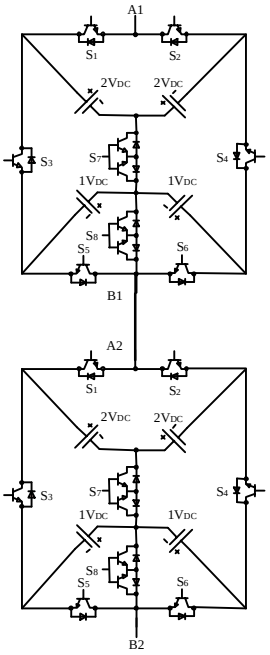


Fig. 4: The first proposed cascade topology (two unit).

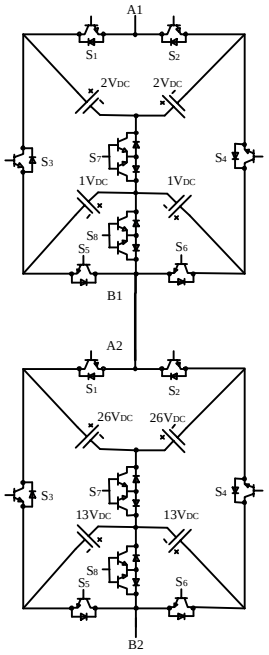


Fig. 5: The second proposed cascade topology (two unit).

In multi-unit cascade connections, there are many redundant switching states used to produce more levels and higher performance by using the second topology. For the second cascade topology, each module has a different amount of DC links in which the first unit has two $1V_{DC}$ and two $2V_{DC}$ DC links and the second unit has two $13V_{DC}$ and two $26V_{DC}$ DC links. These eight DC links can be connected together by different paths to generate more levels than the first cascade topology so that 169 levels can be achieved by the second topology. Figure 5 illustrates the second proposed topology. DC links of each unit are calculated as follows (*n*=number of unit: 2, 3, 4, … and *n*):

Amplitude of lower DC links pair of $unit_n$ = 2 × (the maximum positive level of $unit_{n-1}$) +1

Amplitude of the upper DC links pair of each $unit_n$ = 2 × (Amount of lower DC links of $unit_n$)

Table 4 demonstrates the switching pattern of the second cascade topology from level -84 to level +84. Levels are created by $unit_1$ and $unit_2$. $Unit_2$ creates 0, $\pm 13V_{DC}$, $\pm 26V_{DC}$, $\pm 39V_{DC}$, $\pm 52V_{DC}$, $\pm 65V_{DC}$, $\pm 78V_{DC}$ and $unit_1$ creates 0, $\pm 1V_{DC}$, $\pm 2V_{DC}$, $\pm 3V_{DC}$, $\pm 4V_{DC}$, $\pm 5V_{DC}$, $\pm 6V_{DC}$ for middle levels between levels of $unit_2$.

Table 4: The Switching pattern of the second cascade topology for levels: -84 to +84

Levels	**DC Sources**		**Switching Pattern for $Unit_2$**							
	From $Unit_1$ (*)	From $Unit_2$	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
-84 to -72	($\pm 2V_{DC} \pm 2V_{DC} \pm V_{DC} \pm V_{DC}$)	$-26V_{DC}$ $-26V_{DC}$ $-13V_{DC}$ $-13V_{DC}$	0	1	1	0	0	1	0	0
-71 to -59	($\pm 2V_{DC} \pm 2V_{DC} \pm V_{DC} \pm V_{DC}$)	$-26V_{DC}$ $-26V_{DC}$ $-13V_{DC}$	0	1	1	0	0	0	0	1
-58 to -46	($\pm 2V_{DC} \pm 2V_{DC} \pm V_{DC} \pm V_{DC}$)	$-26V_{DC}$ $-26V_{DC}$	0	1	1	0	1	0	0	0
-45 to -33	($\pm 2V_{DC} \pm 2V_{DC} \pm V_{DC} \pm V_{DC}$)	$-26V_{DC}$ $-13V_{DC}$	0	1	0	0	0	1	1	0
-32 to -20	($\pm 2V_{DC} \pm 2V_{DC} \pm V_{DC} \pm V_{DC}$)	$-26V_{DC}$	0	1	0	0	0	0	1	1
-19 to -7	($\pm 2V_{DC} \pm 2V_{DC} \pm V_{DC} \pm V_{DC}$)	$-13V_{DC}$	1	0	1	0	0	0	0	1
-6 to +6	($\pm 2V_{DC} \pm 2V_{DC} \pm V_{DC} \pm V_{DC}$)	$0V_{DC}$	1	0	1	0	1	0	0	0
+7 to +19	($\pm 2V_{DC} \pm 2V_{DC} \pm V_{DC} \pm V_{DC}$)	$+13V_{DC}$	0	1	0	1	0	0	0	1
+20 to +32	($\pm 2V_{DC} \pm 2V_{DC} \pm V_{DC} \pm V_{DC}$)	$+26V_{DC}$	1	0	0	0	0	0	1	1
+33 to +45	($\pm 2V_{DC} \pm 2V_{DC} \pm V_{DC} \pm V_{DC}$)	$+26V_{DC}$ $+13V_{DC}$	1	0	0	0	1	0	1	0
+46 to +58	($\pm 2V_{DC} \pm 2V_{DC} \pm V_{DC} \pm V_{DC}$)	$+26V_{DC}$ $+26V_{DC}$	1	0	0	1	0	1	0	0
+59 to +71	($\pm 2V_{DC} \pm 2V_{DC} \pm V_{DC} \pm V_{DC}$)	$+26V_{DC}$ $+26V_{DC}$ $+13V_{DC}$	1	0	0	1	0	0	0	1
+72 to +84	($\pm 2V_{DC} \pm 2V_{DC} \pm V_{DC} \pm V_{DC}$)	$+26V_{DC}$ $+26V_{DC}$ $+13V_{DC}$ $+13V_{DC}$	1	0	0	1	1	0	0	0

(*) Switching pattern for $Unit_1$ is based on Table 1

3. NEAREST LEVEL CONTROL (NLC) MODULATION METHOD

As a switching technique, the simplified nearest level control method is used in the proposed modular multilevel inverter [18]. The aim is to use the NLC method in inverter with a high number of levels which can reduce and simplify the calculation of the processor. Figure 6 presents the NLC method pictorially. As shown in Fig. 6a, the controller samples a point from reference voltage (V_{ref}) and then rounds it to the nearest of voltage level (V_{aN}). Each voltage level has a switching logic according to the switching lookup table to change switch status (Fig. 6b). The sampling is repeated for each sample time (T_s).

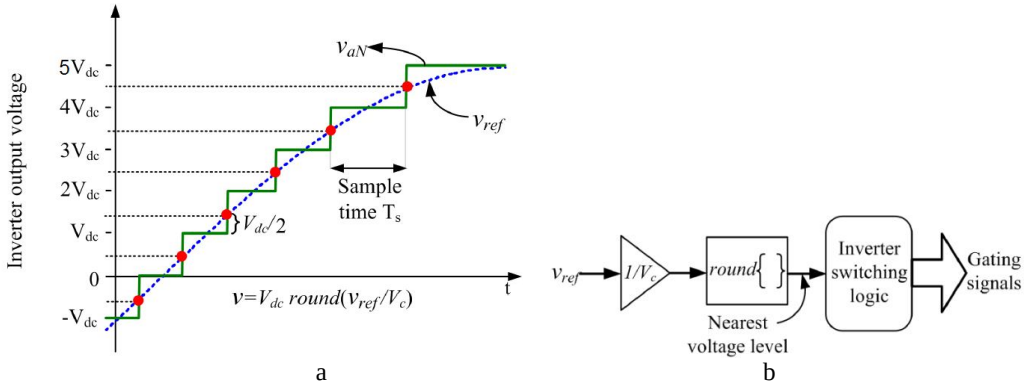


Fig. 6: Nearest level control (a) waveform synthesis (b) control diagram.

4. SIMULATION RESULTS

The proposed multilevel inverter is simulated using MATLAB/SIMULINK to examine the performance of the proposed module. Figure 7 shows the output voltage of 13-levels for the proposed multilevel inverter with NLC switching technique. Each level (V_{DC}) is 50 volts. THD% is calculated 3.87% by FFT analysis for waveform of Fig. 7 which satisfied IEEE519 (i.e max. of THD%: 8%).

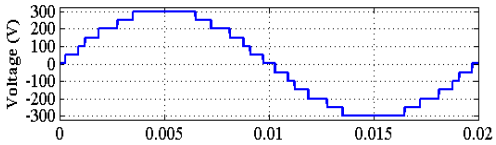


Fig. 7: The waveform of output voltage for the proposed module (simulation).

Figures 8 and 9 depict the results of the first and the second cascade topologies with the NLC switching technique. They confirm the performance and modular abilities of proposed topologies as 25 levels with THD=1.99% for the first cascade topology and 169 levels with THD=0.11% for the second cascade topology. Cascade topologies are known to offer good performance in creating waveforms similar to the sinusoidal waveform with low harmonics.

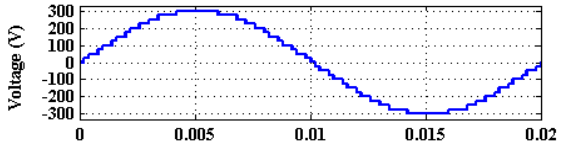


Fig. 8: The waveform of output voltage for the first cascade topology (25 levels) (simulation).

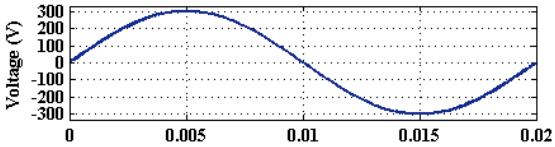


Fig. 9: The waveform of output voltage for the second cascade topology (169 levels) (simulation).

5. EXPERIMENTAL RESULTS

A sample prototype was built in the laboratory to validate the basic proposed module and modular connections with consideration of the limitations in laboratory facilities. Each level is considered 50 volts; thus, there are two 50 volts and two 100 volts DC sources for modules. IGBT 12N60A4, Diode RHRP15120 are used in the laboratory model. Microcontroller ATMEGA16A creates a pulse for switches and HCPL3120 drives IGBTs (Fig. 10). Figure 11 shows the experimental setup in laboratory. The output of the one module (Fig. 3) is a 50 Hz sinusoidal waveform shown in Fig. 12. Also, Fig. 13 depicts output voltage waveform for the first cascade topology (Fig. 4) with 25 levels. Experimental THD is 4.94% and 2.05% for 13 levels and 25 levels, respectively. As the comparison of Fig. 12 and Fig. 13a indicates, the voltage waveform with 25 levels is more similar to a sinusoidal waveform. Also, Fig. 13b and Fig. 13c shows the voltage waveform

of each unit for the cascade topology. The cascade topology shows greater quality with higher waveform resolution and its peak to peak voltage (V_{p-p}) reaches 1.2 KV against V_{p-p} of 13 levels voltage waveform, which is 0.6 KV. Consequently, the experimental test results based on module and cascade topologies show good performance to get more and higher levels by this creative topology.

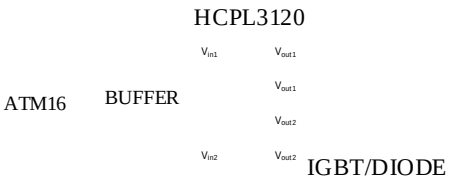


Fig. 10: Schematic of laboratory configuration.

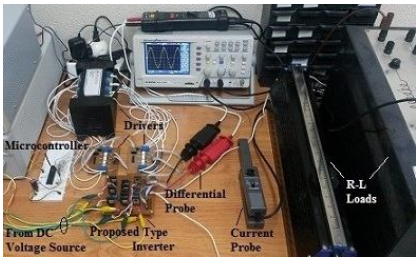
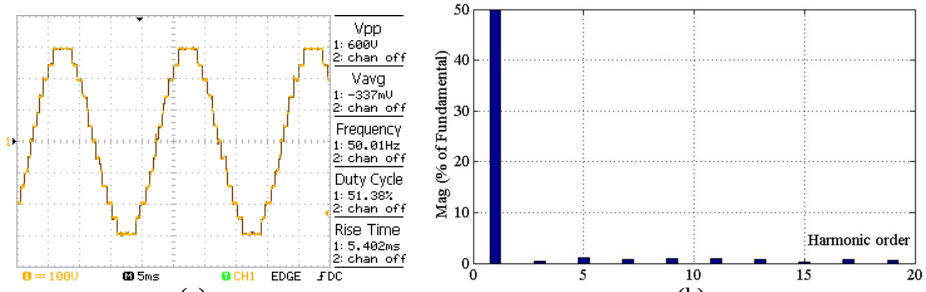
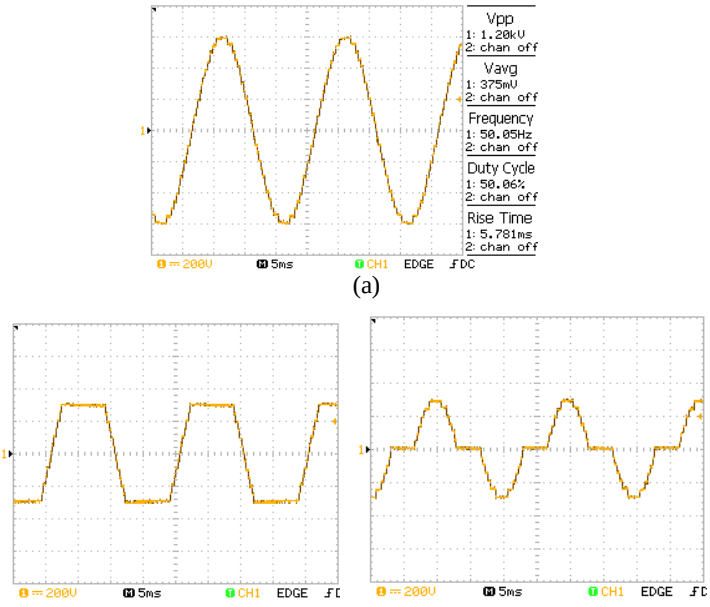


Fig. 11: Picture of experimental setup in laboratory.



(a) (b)

Fig. 12: The output voltage of the proposed multilevel for the base module (a) and spectral analysis (b), 13-level (experimental test).



(a)

(b) (c)

Fig. 13: The output voltage for the first cascade topology in the proposed multilevel (two unit), 25-Level (experimental test) (a) output voltage waveform in Fig. 4 (b) for unit1 in Fig. 4 (c) for unit2 in Fig. 4.

6. CONCLUSION

Nowadays, DC systems and DC sources are widespread. Power quality is the most important quality of these systems for the connection of DC-AC systems. Inverters are coupled with devices of DC-AC connections. This paper presented two new topologies of the multilevel inverter by a new proposed module. The proposed module creates 13 levels of voltage waveform through reduced components. It can be used in high voltage/power and using in DC systems (PV, FC, Battery, DFIG, and HVDC), because the module is able to easily be set in a cascade arrangement and offers low switching frequency for good design. Two cascade topologies are presented for more voltage levels in which the first cascade topology generated 25 levels and the second method generated 169 levels using just two units. Thus, it has a lower construction cost than similar topologies. It does not need any H-bridge circuit and harmonic filter at output. THD% obtained 3.87% and 4.94% in simulation and experimental results for the proposed module respectively, that satisfy harmonics standard (IEEE519). Also, THD% of the first cascade topology calculated 1.99% and 2.05% in simulation and experimental results by the FFT analysis. The second topology has THD%=0.11% by 169 levels.

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