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COMPREHENSIVE ANALYSIS OF A BRIDGED-T PRE-EQUALIZER CIRCUIT FOR HIGH-SPEED VISIBLE LIGHT COMMUNICATIONS

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ABSTRACT: This paper presents a comprehensive analysis of a bridged-T equalizer circuit (BTEC) designed for a high-speed visible light communications (VLC) system. The circuit is proposed to overcome the bandwidth limitation of light-emitting diodes (LEDs) in the VLC system. The advanced design system (ADS) and MATLAB were integrated to analyze the behavior of the BTEC in terms of transfer functions and scattering parameters $S11$, $S12$, $S21$, and $S22$. The results indicate a good correlation between the two tools, with the center frequency being 786 MHz. The 3-dB lower and upper cut-off frequencies are 501 MHz and 1.23 GHz, respectively. The impedance point is at magnitude 1 and 0 phase degrees on the Smith chart. This precise point ensures optimal matching to 50 Ω of source and load impedance. This simulation proves that the bridged-T pre-equalizer circuit is a symmetric and reciprocal network since $S11 = S22$ and $S12 = S21$. This work combines the computational capabilities of MATLAB with the circuit simulation capabilities of ADS, which satisfied the pre-equalizer circuit experimental stage.

ABSTRAK: Kertas kerja ini membentangkan analisis komprehensif bagi litar penyama T terjepit (BTEC) yang direka untuk sistem komunikasi cahaya nampak (VLC) berkelajuan tinggi. Litar ini dicadangkan untuk mengatasi had lebar jalur diod pemancar cahaya (LED) dalam sistem VLC. Sistem reka bentuk lanjutan (ADS) dan MATLAB telah disepadukan untuk menganalisis kelakuan BTEC dari segi fungsi pemindahan dan parameter serakan $S11$, $S12$, $S21$, dan $S22$. Keputusan menunjukkan korelasi yang baik antara kedua-dua alat, dengan frekuensi tengah ialah 786 MHz. Frekuensi potong bawah dan atas 3-dB ialah 501 MHz dan 1.23 GHz, masing-masing. Titik impedans adalah pada magnitud 1 dan 0 darjah fasa pada carta Smith. Titik tepat ini memastikan padanan optimum kepada 50 Ω sumber dan galangan beban. Dalam simulasi ini, terbukti bahawa litar pra-penyamaan bridged-T adalah rangkaian simetri dan timbal balik sejak $S11 = S22$ dan $S12 = S21$. Kerja ini menggabungkan keupayaan pengiraan MATLAB dengan keupayaan simulasi litar ADS, yang memenuhi peringkat percubaan litar pra-penyamaan.

KEYWORDS: *Bridged-T circuit, Pre-equalizer, VLC, Scattering parameter, Two-port networks, and ADS/ MATLAB*

1. INTRODUCTION

Visible light communications (VLC) have been recognized as one of the enablers that could revolutionize the future of wireless communications. The extensive deployment of light-emitting diodes (LEDs) provides dual illumination and communication functionality, particularly in indoor environments [1], [2]. The LED-based VLC system complements radio frequency (RF) wireless systems due to its low cost, energy efficiency, and reliable wireless connectivity solution to meet the infrastructure trends of the 6G networks. However, VLC suffers severely from the limited modulation bandwidth of LEDs, B_{LED} (less than 5MHz for commercial white LEDs) [3], which is lower than the current wireless-fidelity (WIFI) data throughput [4]. Researchers are trying to improve the B_{LED} by employing various techniques in hardware and algorithms, including blue filtering at the receiver (Rx) to filter out the yellow element [5], micron-sized LEDs [6], and advanced modulation schemes, such as orthogonal frequency division multiplexing (OFDM) [7], and pulse amplitude modulation (PAM) [8], and carrier-less amplitude phase (CAP) modulation [9]. However, most mitigation techniques have the limitations of higher implementation complexity, larger fabrication size, higher power consumption, and high costs [3], [10].

Equalization techniques have been employed in various fields, such as audio systems [10], communication systems [11], optical fiber communication [12], and optical wireless communications (OWC) [13]. Equalization is an approach to adjust the balance between the frequency components of a signal, achieved by amplifying or attenuating specific frequency components within an electronic signal [1]. The equalization technique may be performed either at the transmitter (Tx) (i.e., pre-equalization) or the Rx (i.e., post-equalization) using software and hardware approaches. Theoretically, pre-equalization aims to diminish low-frequency components and amplify high-frequency components, achieving a more uniform distribution of the entire received spectrum to enhance system performance [14]. In contrast, post-equalization is performed at the Rx to compensate for other channel losses and mitigate linear/nonlinear distortions [4].

A bridged-T pre-equalizer circuit (BTEC) is used in communication systems to compensate or equalize the frequency-dependent attenuation or distortion introduced by transmission channels. The circuit is typically employed in high-speed data communication, wired or wireless communication systems, audio and video transmission systems, and RF communication systems. The BTEC comprises passive components connected in a specific configuration, including resistors (R), capacitors (C), and inductors (L). The circuit shapes the system's frequency response power booster and attenuates specific frequency components to achieve desired signal characteristics [1].

Huang et al. [15] were the first to demonstrate that a single bridged T network exhibits constant characteristic impedance and consistent response for high-speed and high-frequency applications such as fiber optic communication systems, digital video broadcasting, and voice-over IP (VoIP). The research was then continued by [16] cascading two constant resistance symmetrical bridged-T networks to give more precise channel compensation, which proved that the 3-dB bandwidth was extended from 12 MHz to 235 MHz and subsequently [17] extended from 17 MHz to 366 MHz using a differential output PIN Rx and a blue filter. Next, Nan Chi et al. [9] investigated cascaded homogeneous and heterogeneous BTEC to enhance transmission data rates in a high-speed LED-based VLC system. They found that a 2-cascaded heterogeneous equalizer provides a larger, more significant gain area than a 2-cascaded homogeneous equalizer. The gain values were 21 and 31 dB for heterogeneous and homogeneous designs, respectively. It shows that increasing the gain area affects the magnitude response due to the amplification of the signal. Moreover, Haiqi et al. [18] extended the B_{LED}

used in the VLC system from 14 MHz to 520 MHz with a cascaded BTEC in a real-time indoor environment. Aiming for a simpler single circuit, Ziying et al. [7] achieved 879.2 MHz and 765.2 MHz for the forward transmission parameter $S21$ in simulation and measurement, respectively. Recently, Chengyu et al. [5] demonstrated a novel hybrid pre-equalization circuit to extend the bandwidth of the VLC system from 30 MHz to 600 MHz using a single commercially available phosphorescent white LED. The equalization circuit was based on four cascaded BTECs, an impedance-matching network, and an active RC frequency-selecting network. However, the circuit complexity contributes to higher costs due to high power consumption. In [19], Yufen et al. combined the folded equalization circuit and the bridged-T equalizer, without using blue filters to extend from a few megahertz to 893 MHz. They designed an AC-coupled drive circuit to provide a constant current of 350 mA to the 1 W LED. This VLC system achieved 1.9 Gb/s using OOK-NRZ modulation over a distance of 7 meters, with a bit error rate (BER) of 3×10^{-5}.

While there have been several reports in the literature on enhancing the data rates of VLC systems using BTEC, fewer researchers have analyzed the circuit design in terms of the circuit transfer function and scattering parameters (S-parameters). Furthermore, simple circuits with no active component have lower power dissipation, making them more energy efficient [10]. Hence, this paper focuses on designing a low-complexity pre-equalizer based on a BTEC to enhance the 3-dB bandwidth of the VLC system using the circuit transfer function and S-parameters. The study also aims to optimize the B_{LED} system design while minimizing the circuit complexity using bridged-T networks in pre-equalization circuits for VLC applications.

2. THE BRIDGED-T PRE-EQUALIZER CIRCUIT (BTEC)

A BTEC is an electronic circuit component that is widely used in telecommunications and RF systems. The BTEC consists of a T-network configuration, a type of circuit with a fourth branch connecting the two series arms from input to output terminal ports. Equalization is a well-known method that modifies the stability between the frequency components of a signal by strengthening or weakening, which modifies the amplitude or phase response of specific frequency ranges [1]. Specifically, a pre-equalizer circuit attenuates low-frequency components and amplifies high-frequency components to flatten the entire receiving spectrum, thereby improving the system's performance [14].

2.1. Principles of the Bridged-T Network

Fig. 1 shows the proposed single BTEC, which consists of four equivalent impedances, Z_1, Z_2, Z_3, and Z_4. Referring to Fig. 1(a), Z_1 is the equivalent impedance of $C_1, L_1\, R_1$ whereas the Fig. 1(b) is the equivalent impedance of $C_2, L_2\, R_4$. In order to match the impedance of the input and output ports, this branch bridges the two impedances of Z_2 and Z_3, which corresponds to the desired iterative impedance of the network, R_o = 50 Ω. The input and output voltages are V_{in} and V_{out}, respectively. The circuit was benchmarked by Huang et al. [1]. However, the parameter values and the locations of resistors, in particular R_1 and R_4 exhibit crucial variations that significantly affect the BTEC frequency and phase responses. These variations have led to noteworthy research discoveries.

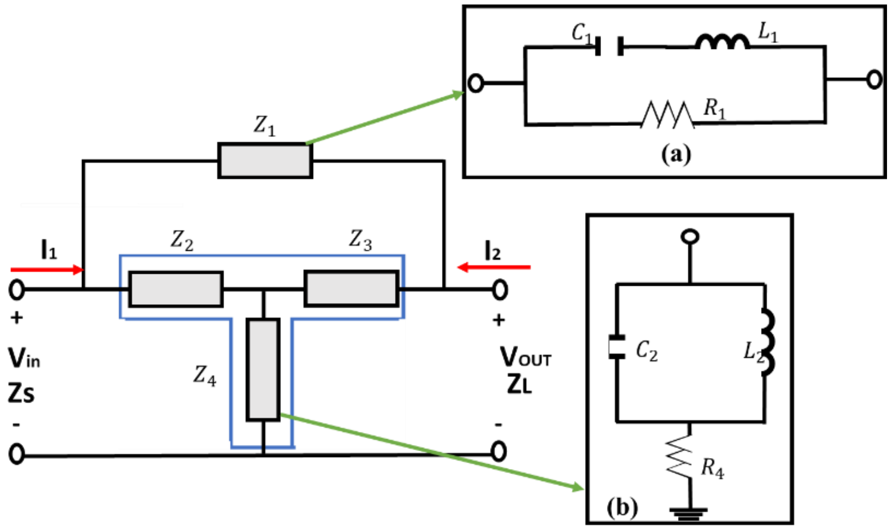

Figure 1. The proposed single bridged- T pre-equalizer circuit.

Additionally, based on Eq. (1) in [15], it can be observed that the transfer function of a single bridged-T network, H_{EQ} which is expressed as:

$$H_{EQ} = \frac{Z_3Z_2 + Z_1Z_4 + Z_3Z_4 + Z_4Z_2}{Z_1Z_2 + Z_3Z_2 + Z_4Z_2 + Z_1Z_4 + Z_3Z_4}, \quad (1)$$

Then, to design a constant resistance amplitude equalizer, the equivalent impedance product of Z_1 and Z_4 must equal R_O^2, which can be expressed as:

$$Z_1 = \frac{R_1\,(Z_c + Z_L)}{R_1 + Z_c + Z_L}, \quad (2)$$

$$Z_4 = R_4 + \frac{Z_c Z_L}{Z_c + Z_L}, \quad (3)$$

$$Z_1 \times Z_4 = R_0^2\,, \quad (4)$$

where $Z_L = j\omega L$, $Z_c = \frac{1}{j\omega C}$, and ω is the angular frequency.

2.2. *S*-parameters in a Two-port Networks

Two-port networks consist of four terminals. A pair of terminals across which a current (*I*) may enter or exit a network is known as a port. *I* enter one terminal and exit through the other terminal, so the net current entering the port equals zero. Fig. 2 shows the two-port circuits to describe the circuit performance in terms of the voltage (*V*) and *I* at both input and output ports. I_1 current enters terminal ‘a’ and exits terminal ‘b’ of the input ports ‘a and b.’

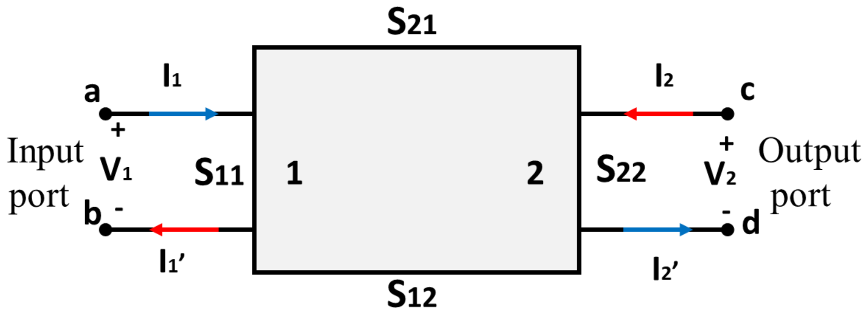

Figure 2. A two-port networks

Fundamentally, $S11$ is the input reflection coefficient, $S12$ is the reverse transmission coefficient, $S21$ is the forward transmission coefficient, and $S22$ is the output reflection coefficient. V_1 is the input voltage from port a-b, while V_2 is the output voltage from port c-d.

The two-port networks describe the circuit's V and I at each port. Hence, it allows us to describe its operation when connected to a more extensive and complex network. The four most prominent parameters are S-parameters, which define the relationship between the incident wave and reflected wave at both ports 1 and 2, Z-parameters (impedance parameters), $ABCD$-parameters (transmission parameters), Y-parameters (admittance parameters), and H-parameters (hybrid parameters).

At high frequencies, which are larger than 300 MHz, such as microwaves, radar waves, and up to GHz frequencies, Ohm's Law is unsuitable for analysing circuit behaviours. Instead, the transmission line theory is preferable due to the causal relationship between the transfer function and S-parameter analysis [20]. The S-parameters knowledge is vital in describing circuit behaviours in high-speed applications, especially in RF and microwave filter design, circuitry and systems, semiconductor device characterization, and high-speed digital systems.

This work calculates the S-parameters with MATLAB and simulates them with ADS software. The default source and load impedances in ADS are 50 Ω. Additionally, the proposed design is derived by analysing the parallel interconnection of two port networks in terms of the S-parameters, including $S11$, $S12$, $S21$, and $S22$.

The BTEC was considered as a parallel interconnection of the two port networks, represented using Y-parameters as shown in Fig. 1. The input and output ports are Z_s and Z_L, respectively, and concurrently Z_s represents the output impedance of the vector network analyser (VNA) and Z_L represents the load of the circuit. The network admittance, Y_1 is solely for Z_1, can be expressed as:

$$Y_1 = \begin{bmatrix} \frac{1}{Z_1} & -\frac{1}{Z_1} \\ -\frac{1}{Z_1} & \frac{1}{Z_1} \end{bmatrix}, \tag{5}$$

The T-shape configuration of Z_2, Z_3, and Z_4 , the network admittance Y_2 , is expressed as:

$$Y_2 = \begin{bmatrix} \frac{Z_3 + Z_4}{Z_2Z_3 + Z_2Z_4 + Z_3Z_4} & -\frac{Z_4}{Z_2Z_3 + Z_2Z_4 + Z_3Z_4} \\ -\frac{Z_4}{Z_2Z_3 + Z_2Z_4 + Z_3Z_4} & \frac{Z_2 + Z_4}{Z_2Z_3 + Z_2Z_4 + Z_3Z_4} \end{bmatrix}, \tag{6}$$

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The total admittance, Y_T can be expressed as:

$$Y_T = Y_1 + Y_2 \,, \tag{7}$$

where Z_1 and Z_4 same as in Eqs (1) and (2), while $Z_2 = Z_3 = R_o$.

The S-parameters and the normalized Y-parameters with Z_s and, Z_L can be expressed as [21]

$$S11 = \frac{\left[1 - Y_{11n}\left(\frac{Z_s^*}{Z_s}\right)\right](1 + Y_{22n}) + Y_{12n}Y_{21n}\left(\frac{Z_s^*}{Z_s}\right)}{(1 + Y_{11n})(1 + Y_{22n}) - Y_{12n}Y_{21n}}, \tag{8}$$

$$S12 = \frac{-2Y_{21n}}{(1 + Y_{11n})(1 + Y_{22n}) - Y_{12n}Y_{21n}}, \tag{9}$$

$$S21 = \frac{-2Y_{21n}}{(1 + Y_{11n})(1 + Y_{22n}) - Y_{12n}Y_{21n}}, \tag{10}$$

$$S22 = \frac{(1 + Y_{11n})\left[(1 - Y_{22n})\left(\frac{Z_L^*}{Z_L}\right)\right] + Y_{12n}Y_{21n}\left(\frac{Z_L^*}{Z_L}\right)}{(1 + Y_{11n})(1 + Y_{22n}) - Y_{12n}Y_{21n}}, \tag{11}$$

where the normalized admittance parameters are denoted as:

$$Y_{11n} = \frac{Y11}{Z_s}\,; Y_{12n} = Y_{12}\sqrt{Z_s \times Z_L}\,; Y_{21n} = Y_{21}\sqrt{Z_s \times Z_L}\,; \text{and } Y_{22n} = \frac{Y22}{Z_L}.$$

2.3. Relationship of Transfer Function and S-parameter

The transfer function and S-parameters are crucial mathematical models for comprehending the systems and network performance. Although both models serve the same purpose, they provide distinct information about the system's response. The transfer function characterizes the system's input-output relationship, specifically in the frequency domain. Whereas S-parameters describe the power transfer and scattering characteristics of a network or device[20].The $S21$ of a single equalizer circuit can be expressed as:

$$S21 = 2 \times \mathrm{H_{EQ}} \,, \tag{12}$$

where $\mathbf{H_{EQ}}$ is the frequency response of a single equalizer.

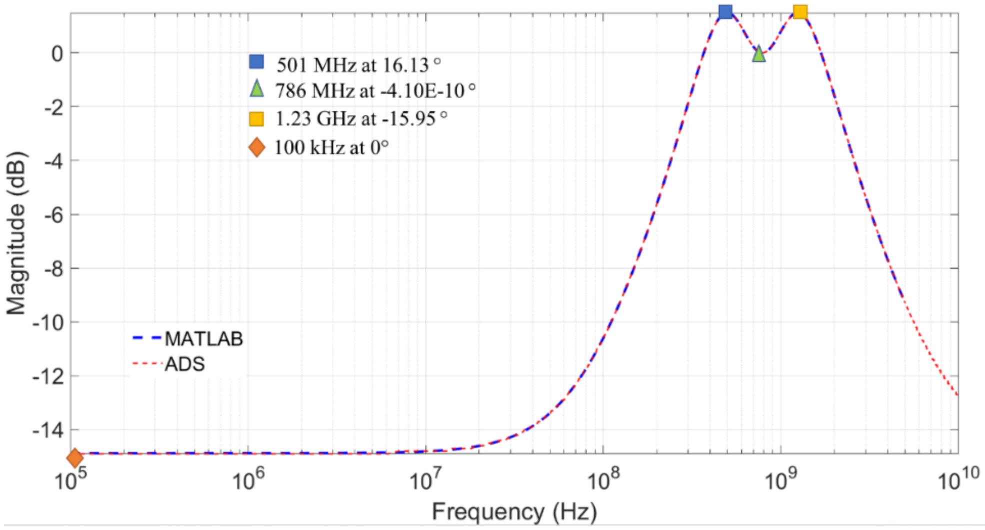
In this paper, both MATLAB and ADS results are then compared for validation. The comparison of the obtained output with the theoretical model ascertains the validity of the proposed design and ensures its practicality and feasibility.

3. RESULTS AND DISCUSSION

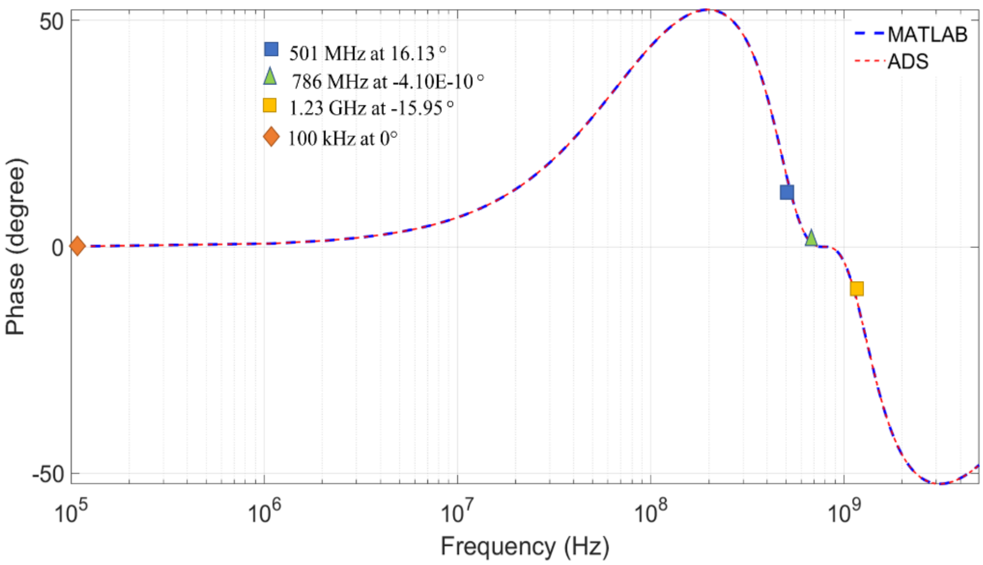
This section describes the simulation results of the pre-equalizer circuit through cross-validation analysis using MATLAB and ADS. The analysis compares the frequency response of the transfer function and S-parameter analysis for validation purposes. The process was initiated by adjusting the component values using Eq. (4) through MATLAB simulation. Following this adjustment, the circuit was constructed using ADS software using the identified optimal values. Upon identifying the optimal values in ADS software, the closest available component values were selected in our laboratory. In this work, the component values are set to $R_1 = 500\ \Omega$, $R_4 = 5\ \Omega$, L = 10 nH, C = 4.1 pF, Z_2 and Z_3 = 50 Ω. The value of R_1 is obtained from ADS simulation, and R_4 is calculated from Eq (3). Additionally, to maintain the impedance stability of the two-port circuit, the values of $C_1 = C_2$ and $L_1 = L_2$.

3.1. The Frequency Response of the Transfer Function

Fig. 3 presents the transfer function responses versus frequency from both MATLAB and the ADS simulation tools. The MATLAB result is based on the calculation using Eq (1), whereas the ADS simulation result is obtained from the output voltage to input voltage ratio in the proposed design.



(a) The magnitude response



(b) The phase response

Figure 3. Comparison of (a) magnitude response and (b) phase response of the pre-equalizer circuit using MATLAB and ADS.

Fig. 3 (a) shows the frequency response result, which shows the maximum amplitude of 1.48 dB gain at double peak responses of 501 MHz and 1.23 GHz. The presence of a double

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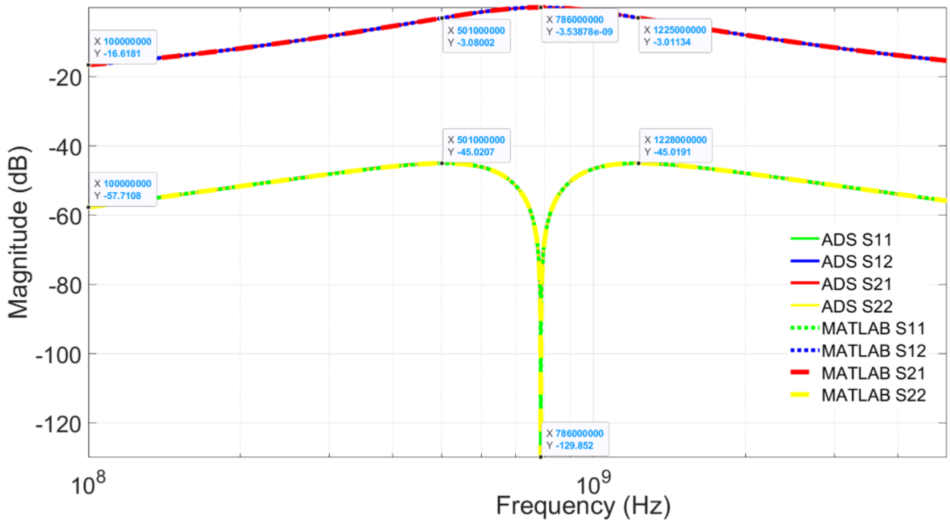
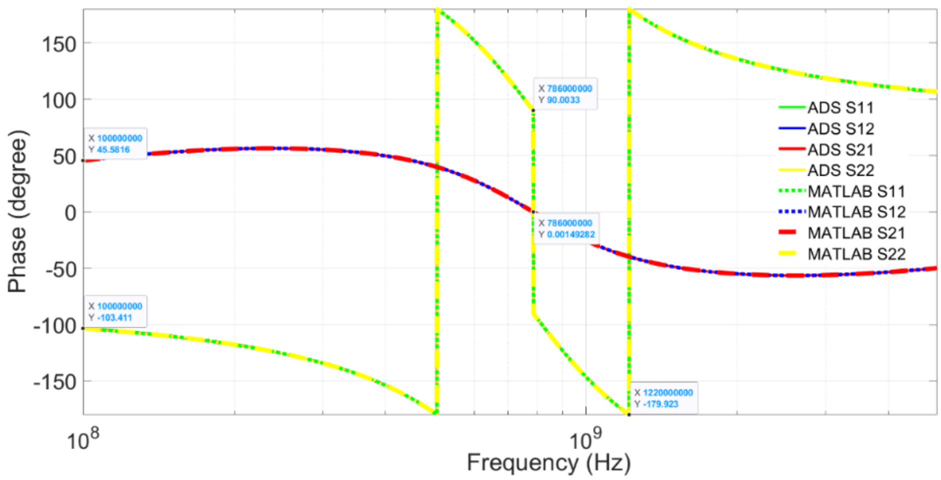
peak in the frequency response curve resulting from the resonant circuit configuration of R, L, and C, each at Z_1 and Z_4, enhances the selectivity and precision of filtering in the passband. The center frequency was 786 MHz at 0 dB, indicating that the input signal was neither amplified nor attenuated. This allowed for the preservation of the original signal strength at the center frequency while attenuating the lower and upper cut-off frequencies. The minimum attenuation was -14.9 dB at 100 kHz, demonstrating that the BTEC attenuates frequencies outside the passband by at least -14.9 dB. Fig. 3 (b) shows that the phase response of both the calculated and simulated results was identical, providing evidence of the circuit design accuracy and consistency of the simulation tools and mathematical methods.

3.2. Scattering Parameter Analysis

To investigate the proposed BTEC's performance in the frequency domain, the start and end sweep frequencies were set to 100 MHz and 5 GHz, respectively, with 1 MHz increment for both calculation and simulation. Fig. 5. illustrates the S–parameters in terms of magnitude and phase response calculated using MATLAB and simulated with the ADS tool, respectively.



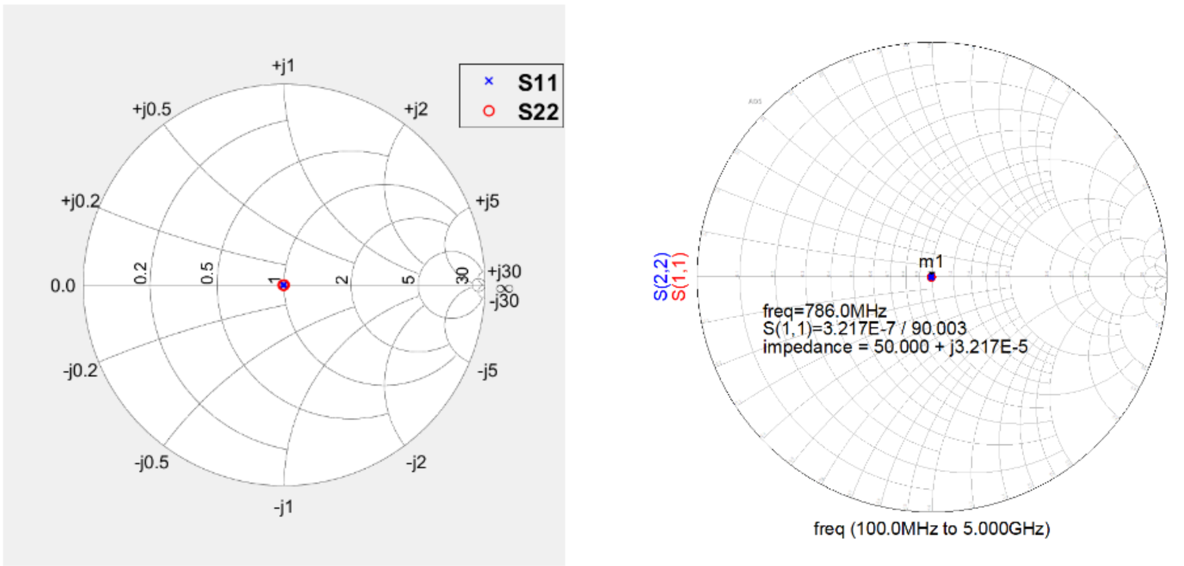
(a) Magnitude responses



(b) Phase responses

Figure 4. Simulated ADS and calculated MATLAB in terms of (a) magnitude response and (b) phase response over frequency.

In Fig. 4 (a), the obtained center frequency was 786.1 MHz at -16.62 dB with a 3-dB lower cut-off frequency of 501 MHz and a 3-dB upper cut-off frequency of 1.23 GHz, which resulted in a bandwidth of 729 MHz. In Fig. 4 (b), it can be observed that the phase angle was 0 degrees at the center frequency in calculation and simulation, which indicates that the BTEC did not introduce any additional phase shift. This means that the output signal was in phase with the input signal. The calculated and simulated results confirmed that the S11 and S22 responses were identical, while the S12 response was identical to S21. The similarity of ADS and MATLAB results proved that BTEC is a symmetric and reciprocal network. This finding validated that the circuit was investigated correctly through calculation and simulation.



(a) MATLAB (b) ADS

Figure 5. S11 and S22 on the Smith chart

The BTEC input and output reflection coefficients, S11 and S22 parameters, were plotted on the Smith chart using MATLAB and ADS, as shown in Fig. 5 (a) and (b), respectively. The circuit demonstrated highly effective matching of the source and load impedances, as evidenced by the plots produced in both software. The center point of the Smith chart, with a magnitude of 1 and 0 degrees, clearly indicates that BTEC delivers excellent impedance matching. Moreover, the calculated and simulated results showed good agreement in matching the source and load impedance to the standard 50 Ω.

Table 1 summarizes the proposed circuit with the bridged-T circuit in the VLC system. Remarkably, for a single BTEC method, our designed pre-equalizer circuit outperformed the research presented in [15] and [7]. The proposed BTEC and the work in [15] shared the same total number of passive components: 2 inductors, 2 capacitors, and 4 resistors, with a peak response of 175 MHz. In contrast, the work presented in [7] utilizes a lesser number of passive components, but the simulation and measurement results were significantly higher, at 879.2 MHz and 765.2 MHz, respectively. However, it is noted that neither work validated the circuit transfer function through analytical and simulation modeling. The discussion in both works was limited to the presentation of the S21 and S22 scattering parameters, as obtained through simulation and measurement.

Table 1. Comparison of the BTEC employed in pre-equalization in the VLC system

Papers	Light device	BTEC Methods	f_c (MHz)	H_{EQ}	*S*-param	3-dB VLC
[15]	RGB (Cree)	single	175 MHz	Derived, no validation	*S*21; *S*22 (both)	-
[16]	white LED (OSRAM)	2- cascaded	353 MHz	Derived, no validation	*S*21 (M)	12MHz to 235 MHZ
[17]	white LED (OSRAM)	2- cascaded	352 MHz	Derived, no validation	*S*21 (M)	17MHz to 366MHz
[9]	RGB (Engine)	2- cascaded	400 MHz	-	*S*21 (S)	-
[18]	white LED (OSRAM)	RC-series parallel cascaded	-	Derived, no validation	-	1 MHz to 520 MHz
[7]	HV-Blue LED	single	879.2 MHz (S) 765.2 MHz (M)	Derived, no validation	*S*21; *S*22 (both)	45 MHz to 750 MHz S21 (air)/ to 850 MHz (underwater)
[5]	white LED (OSRAM)	4- cascaded	-	Yes	*S*21 (M)	30 MHz to 600 MHz
[19]	white LED (OSRAM)	2- cascaded	-	Derived, no validation	-	893 MHz
This paper	white LED (OSRAM)	single	786 MHz (S)	Yes	*S*11; *S*12; *S*21; *S*22 (both)	Expected to reach 800 MHz

S = simulation; *M* = measurement; f_c=center frequency; *S*-param = scattering parameter; RGB = red, green, blue.

In this work, the frequency-domain characterization of the circuit's behavior is well described through the analytical and simulation models of the S11, S21, S21, and S22 scattering parameters. This comprehensive analysis ensures good impedance matching, stability, and overall validation of the circuit's performance in high-frequency applications.

4. CONCLUSION

In this paper, we analyzed the performance of a pre-equalizer circuit based on a bridged-T network. The findings demonstrate an excellent alignment between the calculated and simulated results, which were performed using MATLAB and ADS software. We successfully achieved a center frequency of 786 MHz, designed with a single bridged-T circuit configuration. The 3-dB lower and upper cut-off frequencies obtained were 501 MHz and 1.23 GHz, respectively. Besides, we have demonstrated that *S*11=*S*22 and, likewise, *S*12 = *S*21, indicating that the circuit is a symmetric and reciprocal network. The circuit is designed to support a port impedance of 50 Ω port, making it compatible with a range of devices, including amplifiers, RF connectors, and cables. In comparison to previous works, our findings show a significant improvement in terms of center frequency f_c and 3-dB cut-off frequencies. Notably, the utilization of a single bridged-T circuit has resulted in reduced circuit complexity and lower fabrication cost. Additionally, both *S*-parameters and frequency response analysis are essential parameters in comprehending the system's frequency-related behavior despite their fundamental disparities. These findings are critical for validating the proposed design and ensuring its efficacy during the experimental stage.

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