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ANALYTICAL MODEL OF SUBTHRESHOLD SWING FOR JUNCTIONLESS DOUBLE GATE MOSFET USING FERROELECTRIC NEGATIVE CAPACITANCE EFFECT

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ABSTRACT: An analytical Subthreshold Swing (SS) model is presented to observe the change in the SS when a stacked SiO_2-metal-ferroelectric structure is used as the oxide film of a JunctionLess Double Gate (JLDG) MOSFET. The SS of 60 mV/dec or less is essential to reduce power dissipation while maintaining transistor performance. If a ferroelectric material with Negative Capacitance (NC) effect is used, the SS can be reduced below 60 mV/dec. The analytical SS model of the ferroelectric NC FET presented to analyze this was in good agreement with the SS derived from the relation between the drain current and gate voltage, using 2D potential distribution. As results were derived from the analytical SS model, it was found that it is possible to obtain an SS of 60 mV/dec or less even at 15 nm channel length by adjusting the thicknesses of the silicon channel, SiO_2, and ferroelectric. In particular, the change in SS according to the ferroelectric thickness was saturated as the thickness of SiO_2 increased and was almost constant as the thickness of the silicon channel decreased.

ABSTRAK: Model Ayunan Subambang (SS) analitikal dibentangkan bagi melihat perubahan pada SS apabila struktur feroelektrik-logam-SiO_2 bertindan digunakan sebagai filem oksida bagi MOSFET Dua Get Tanpa Simpang (JLDG). SS 60 mV/dec atau kurang adalah penting bagi mengurangkan pelesapan kuasa sambil mengekalkan prestasi transistor. Jika bahan feroelektrik dengan kesan Kapasitans Negatif (NC) digunakan, SS dapat dikurangkan bawah 60 mV/dek. Model SS analitikal feroelektrik NC FET yang digunakan bagi kajian ini adalah sesuai dengan SS yang diperoleh daripada hubungan antara arus serapan dan voltan get, menggunakan edaran potensi 2D. Dapatan terbitan melalui model SS analitikal, mendapati bahawa adalah mungkin bagi mendapatkan SS pada 60 mV/dek atau kurang walaupun panjang laluan adalah 15 nm dengan melaraskan ketebalan saluran silikon, SiO_2, dan feroelektrik. Terutama apabila perubahan ketebalan feroelektrik SS adalah tepu ketika ketebalan SiO_2 meningkat, dan hampir malar apabila ketebalan saluran silikon berkurang.

KEYWORDS: *subthreshold swing; junctionless; ferroelectric; negative capacitance; double gate*

1. INTRODUCTION

In the competition for miniaturization of transistors, high-speed operation and low power consumption are essential. However, the recent scaling theory according to Moore's law is no longer followed by the power consumption generated during the switching process [1-3]. For low power consumption, the supply voltage must be reduced while maintaining high on-

current. However, a decrease in the supply voltage requires a decrease in the threshold voltage, which causes an increase in parasitic current and static power dissipation [4]. A way to solve the trade-off relationship between power consumption and transistor performance is to reduce the Subthreshold Swing (SS). According to Boltzmann Tyranny [5], the body factor of conventional MOSFETs is greater than 1. A device developed to reduce the SS by making the body factor smaller than 1 is a Negative Capacitance (NC) FET [6-11]. NC FETs show the characteristics such as steep SS and high switching current ratio (I_{on}/I_{off}), and are known as good candidates for low power consumption [12-14]. The material used for the gate oxide film to fabricate the NC FET is a ferroelectric thin film. The NC effect occurs in the region where the ferroelectric polarization increases when the external electric field decreases. However, the NC effect is naturally unstable, and it is used in series with a general capacitor to solve this problem [15]. Therefore, instead of using only ferroelectric material as a gate oxide film, a stacked gate structure of a metal-ferroelectric-insulator-semiconductor (MFIS) structure and a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure is used as shown in Fig. 1 [16-19]. Ultimately, controlling the charge in the channel of the FET using the ferroelectric polarization charge is the core of the NC FET. The organic-ferroelectric, lead (Pb) Zirconate titanate (PZT) of inorganic perovskite structure, $HfZrO_2$, etc. as ferroelectric materials, are used to show NC effect [20-23].

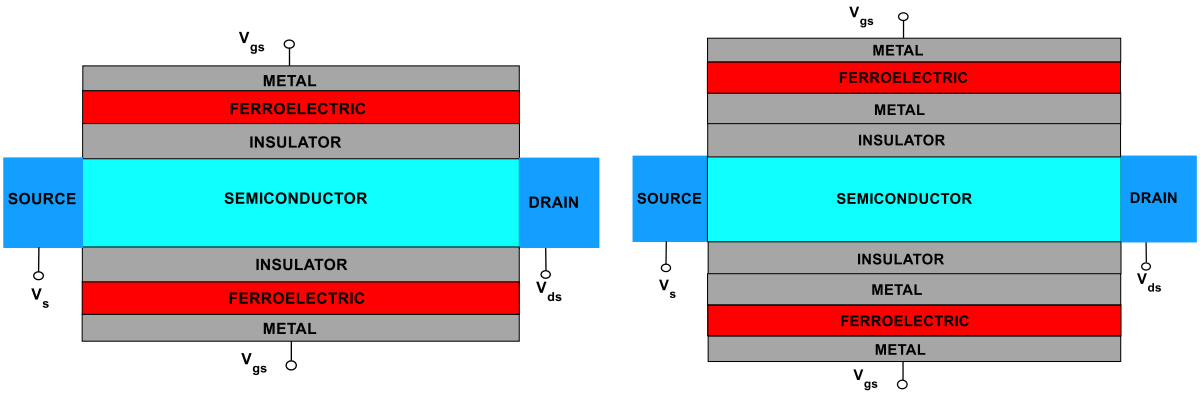

Fig. 1: (a) MFIS and (b) MFMIS structures of DG MOSFET.

In order to reduce the power consumption, the supply voltage must be reduced, but this obstacle must be overcome since the SS is limited to 60 mV/dec to room temperature. To this end, it is necessary to induce the necessary charge in the channel with a gate voltage as small as possible. This can be solved by NC voltage amplification occurring in NC FET using ferroelectric material, and at this time, a steep SS of 60 mV/dec or less can be induced. Rahi et al. [24] reviewed the advantage that the on-current of the NC FET is greater than that of the tunnel FET with a characteristic of 60 mV/dec or less. Alam et al. [25] only reviewed NC FETs with MFIS structure, and Tu et al. [26] presented ferroelectric NC FETs with SS <60 mV/dec. In this paper, we will use the MFMIS structure as the stacked gate structure.

This structure is widely used as a structure to solve the field nonuniformity problem that occurs in the MFIS structure, and Pahwa et al. [27] compared these two structures. In particular, we will observe the reduction effect of SS by using this structure for the gate oxide film of JunctionLess (JL) FET. The JLFET is a structure that can solve the difficulties of processing in the sub-10nm structure by configuring the doping of the source/drain and the channel with the same type and concentration [28-31]. Rassekh et al. [32] applied MFMIS

structure to a JL Double-Gate (DG) FET and observed effects such as gate voltage amplification and DIBL, but did not present an analytical model of SS. Therefore, in this paper, we propose an analytical SS model of JLDG FET with MFMIS gate structure using the potential distribution model of JLDG FET and the relationship between the polarization and free energy of ferroelectric material according to Landau theory [33]. This result will be compared with the SS obtained from the current-voltage characteristic to prove the validity of this analytical SS model.

2. SUBTHRESHOLD SWING MODEL OF FERROELECTRIC NC FET

2.1 The Structure of Ferroelectric NC FET and I-V Characteristics

Figure 2 shows the cross-sectional view of the NC FET of the MFMIS structure used in this paper. The source/drain and channel were equally highly doped with N_d^+, and a symmetrical JL FET with the same upper and lower gates was used. In this paper, $N_d^+=10^{19}/\text{cm}^3$ was used. The voltage applied to METAL2, V_{gs2}, can be expressed as the sum of the voltage induced in METAL1, V_{gs1}, and the voltage across the ferroelectric material, V_f. The V_{gs2} is defined in Eq. (1)

$$V_{gs2} = V_{gs1} + V_f \ . \tag{1}$$

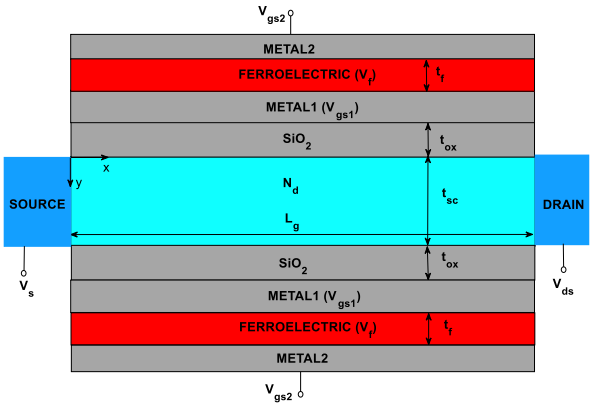

Fig. 2: Schematic diagram of a symmetric JLDG FET with ferroelectric material as the stacked gate oxides.

According to the ferroelectric charge density Q of [34], the voltage across the ferroelectric material, V_f can be expressed as in Eq. (2).

$$V_f = 2\alpha t_f Q + 4\beta t_f Q^3 + 6\gamma t_f Q^5 \tag{2}$$

Here, the α, β, γ can be obtained from the P-E hysteresis curve between the ferroelectric Polarization, P and the Electric Field, E extracted from the ferroelectric capacitor. That is, using the Remanent Polarization, P_r and Coercive Field, E_c in the P-E hysteresis curve, it can be obtained as in Eq. (3) [35].

$$\alpha = -\frac{3\sqrt{3}}{2}\frac{E_c}{P_r}\ (m/F)$$
$$\beta = \frac{3\sqrt{3}}{2}\frac{E_c}{P_r^3}\ (m^5/F/C^2) \tag{3}$$

In this paper, the α and β are found from $P_r = 17\,\mu C/cm^2$ and $E_c = 1.2\,MV/cm$, the experimental results of the HZO film, and $\gamma = 0$ [34]. In order to obtain V_f of Eq. (2), first the charge density of ferroelectric Q must be obtained. To find Q, the charge Q_{sc} in the channel by Rassekh's method [36] is as in Eq. (4).

$$Q_{sc} = -2C_{ox}(V_{gs1} - \Delta\phi_{ms} - \phi_s) \tag{4}$$

where $\Delta\phi_{ms}$ is the work function difference between the metal and the intrinsic semiconductor, ϕ_s is the surface potential, and C_{ox} is the capacitance according to the thickness of SiO_2 used as insulator. The following Poisson equation (5) is used to obtain ϕ_s in Eq. (4).

$$\partial^2\phi(x,y)/\partial x^2 + \partial^2\phi(x,y)/\partial y^2 = -qN_d/\varepsilon_{si} \tag{5}$$

In this case, the following four boundary conditions were used as shown in Eq. (6).

$$\begin{aligned}
&\phi(0,y) = V_s \\
&\phi(L_g,y) = V_s + V_d \\
&\phi(x,0) = V_{gs1} - V_{fb} + \frac{\varepsilon_{si}}{C_{ox}}\frac{\partial\phi}{\partial y}\bigg|_{y=0} \\
&\phi(x,t_{si}) = V_{gs1} - V_{fb} + \frac{\varepsilon_{si}}{C_{ox}}\frac{\partial\phi}{\partial y}\bigg|_{y=t_{sc}},
\end{aligned} \tag{6}$$

where ε_{si} is the dielectric constant of silicon, V_{fb} is the flat band voltage. Using Ding's expansion method [37], the potential distribution can be expressed as in Eq. (7).

$$\phi(x,y) = V_s + \frac{V_d x}{L_g} + \sum_{n=1}^{\infty} A_n(y)\sin\frac{n\pi x}{L_g}, \tag{7}$$

where

$$A_n(y) = C_n e^{k_n y} + D_n e^{-k_n y} - f_n/k_n$$

$$f_n = \begin{cases} -\dfrac{4qN_d}{n\pi\varepsilon_{si}}, & n = 1,3,5,\cdots \\ 0, & n = 2,4,6,\cdots \end{cases}$$

$$C_n = \frac{C_{ox}\left(f_n - G_n k_n^2\right)}{k_n^2\left[\left(C_{ox} + \varepsilon_{si}k_n\right)e^{k_n t_{sc}} + \left(C_{ox} - \varepsilon_{si}k_n\right)\right]}$$

$$D_n = C_n e^{k_n t_{sc}}$$

$$G_n = \begin{cases} \left(\dfrac{2}{n\pi}\right)\left[2\left(V_s - V_{gs1} + V_{fb}\right) + V_{ds}\right], & n = 1,3,5,\cdots \\ 0, & n = 2,4,6,\cdots \end{cases}$$

At this time, the surface potential at $y = 0$ is

$$\phi_s = \frac{V_{ds}}{L_g}x + \sum_{n=1}^{\infty}\left[C_n + D_n - f_n/k_n^2\right]\sin\frac{n\pi x}{L_g}. \tag{8}$$

Substituting Eq. (8) into Eq. (4), the charge in the channel can be found as Eq. (9)

$$\begin{aligned} Q_{SC} &= -2C_{ox}(V_{gs1} - \Delta\phi_{ms} - \phi_s) \\ &= -2C_{ox}\left(V_{gs1} - \Delta\phi_{ms} - \frac{V_{ds}}{L_g}x - \sum_{n=1}^{\infty}\left[C_n + D_n - f_n / k_n^2\right]\sin\frac{n\pi x}{L_g}\right) \end{aligned} \tag{9}$$

The charge Q in the ferroelectric can be obtained from Eq. (10) by calculating the integration of the total charge Q_{SC} existing in the channel over channel length.

$$WL_g \times 2Q = -\int_0^{L_g} WQ_{SC}dx \tag{10}$$

where W is the channel width. Then, the charge Q in ferroelectric is obtained as in Eq. (11).

$$\begin{aligned} Q &= -\frac{1}{2L_g}\int_0^{L_g} Q_{SC}dx \\ &= -\frac{1}{2L_g}\int_0^{L_g}\left\{-2C_{ox}(V_{gs1} - \Delta\phi_{ms} - \frac{V_{ds}}{L_g}x - \sum_{n=1}^{\infty}\left[C_n + D_n - f_n / k_n^2\right]\sin\frac{n\pi x}{L_g})\right\}dx \\ &= \frac{C_{ox}}{L_g}\left[(V_{gs1} - \Delta\phi_{ms})L_g - \frac{V_{ds}}{2}L_g + \sum_{n=1}^{\infty}\left[C_n + D_n - f_n / k_n^2\right]\left(\frac{L_g}{n\pi}\right)\cos\frac{n\pi x}{L_g}\Big|_0^{L_g}\right]. \\ &= C_{ox}\left[(V_{gs1} - \Delta\phi_{ms} - \frac{V_{ds}}{2}) + \sum_{n=1}^{\infty}\left[C_n + D_n - f_n / k_n^2\right]\left(\frac{1}{n\pi}\right)\left[(-1)^n - 1\right]\right] \end{aligned} \tag{11}$$

At this time, by substituting Eq. (11) into Eq. (2), V_f can be obtained.

In order to obtain the drain current for the corresponding gate voltage V_{gs2}, the drain current is obtained from the following Eq. (12) with Eq. (7).

$$I_d = \frac{qn_i\mu_n WkT\left\{1 - \exp\left(\frac{-qV_d}{kT}\right)\right\}}{\int_0^{L_g}\frac{1}{\int_0^{t_{sc}}\exp\left(\frac{q\phi(x,y)}{kT}\right)dy}dx} \tag{12}$$

where k, T, n_i, μ_n and W are Boltzmann's constant, absolute temperature, the intrinsic electron concentration, the electron mobility, and a channel width, respectively.

The relationship between drain current and gate voltage obtained using Eqs. (7) and (12) is shown with the thickness of the ferroelectric material, t_f as a parameter in Fig. 3. The red dotted line in Fig. 3 is the baseline where SS is 60 mV/dec. The SS represents the decrease in the gate voltage when the drain current decreases by one order. As shown in Fig. 3, when observing the change in drain current according to the gate voltage in the subthreshold region at t_f = 0 nm, SS shows a value of 60 mV/dec or higher. As the thickness of the ferroelectric material increases, the slope of the current-voltage curve increases in subthreshold, and it can be found that SS decreases below 60 mV/dec by the definition of SS as shown in Eq. (13). Therefore, the negative charge effect by the ferroelectric material can be observed. In addition, it was observed that the off current representing the drain current at 0 gate voltage also decreased significantly as the thickness of the ferroelectric material increased.

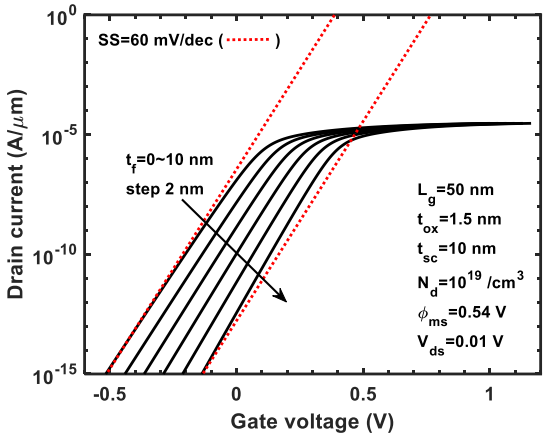

Fig. 3: Drain current vs. gate voltage curves with the thickness of ferroelectric material, t_f as a parameter.

Figure 4 shows the relationship between drain current and gate voltage obtained by using the gate channel length, L_g as a parameter when the thickness of the ferroelectric material, t_f is 10 nm. The red dotted line indicates SS=60 mV/dec in Fig. 4. It is known that there is a significant decrease in SS with increasing channel lengths. As can be seen from Fig. 4, it can be observed that the SS is 60 mV/dec value at about 25 nm of channel length under the conditions indicated inside Fig. 4, and decreases to 60 mV/dec or less as the channel length increases. Also note that the SS is saturated as the channel length increases. When the channel length is decreased to about 15 nm, it can be seen that SS significantly increases even at t_f=10 nm. Of course, as can be seen from Fig. 3, the SS will increase further as t_f decreases. As such, it was observed that a negative capacitance effect occurs due to the presence of ferroelectric thickness t_f, and a SS value of 60 mV/dec or less can be achieved.

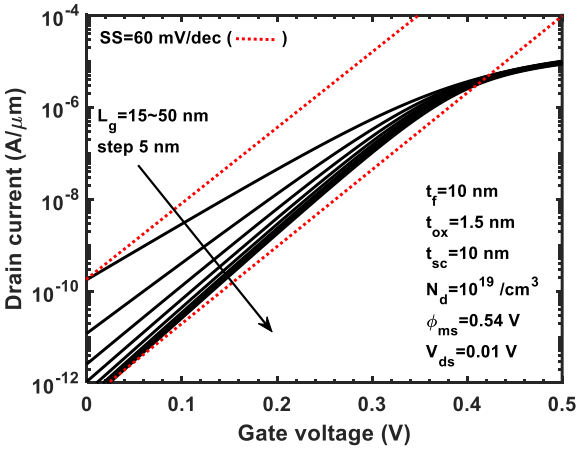

Fig. 4: Drain current vs. gate voltage curve with the channel length L_g as a parameter.

2.2 The Analytical SS Model of Ferroelectric NC FET

We want to derive an analytical model for the SS of ferroelectric NC FETs in this paper. By the definition of SS, the SS can be expressed as in Eq. (13).

$$SS = \frac{\partial V_{gs2}}{\partial \log I_{ds}} = \ln(10)\left(\frac{kT}{q}\right)\left(\frac{\partial \phi_{\min}}{\partial V_{gs2}}\right)^{-1} \tag{13}$$

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In particular, in the case of JLDG FET, most electrons will be conducted through the center, so using Eq. (7), the last parenthesis term of Eq. (13) can be expressed as in Eq. (14).

$$\frac{\partial \phi_{\min}}{\partial V_{gs2}} = \sum_{n=1}^{\infty} \frac{\partial A_n(y)}{\partial V_{gs2}} \sin\left(\frac{n\pi x}{L_g}\right)\Bigg|_{x=x_{\min},\, y=t_{sc}/2} = \sum_{n=1}^{\infty} \frac{\partial A_n(t_{sc}/2)}{\partial V_{gs2}} \sin\left(\frac{n\pi x_{\min}}{L_g}\right) \tag{14}$$

$$\begin{aligned}\frac{\partial A_n(t_{SC}/2)}{\partial V_{gs2}} &= e^{k_n t_{sc}/2} \frac{\partial C_n}{\partial V_{gs2}} + e^{-k_n t_{sc}/2} \frac{\partial D_n}{\partial V_{gs2}} \\ &= e^{k_n t_{sc}/2} \frac{\partial C_n}{\partial V_{gs2}} + e^{-k_n t_{sc}/2} \frac{\partial C_n}{\partial V_{gs2}} e^{k_n t_{sc}} \\ &= e^{k_n t_{sc}/2} \frac{\partial C_n}{\partial V_{gs2}} + e^{k_n t_{sc}/2} \frac{\partial C_n}{\partial V_{gs2}} = 2e^{k_n t_{sc}/2} \frac{\partial C_n}{\partial V_{gs2}}\end{aligned}$$

In Eq. (14), the derivative of C_n with respect to V_{gs2} must first be found. Since C_n is not a direct function of V_{gs2}, the following parametric differential method is used.

$$\frac{\partial C_n}{\partial V_{gs2}} = \frac{\partial C_n}{\partial V_{gs1}} \frac{\partial V_{gs1}}{\partial Q} \frac{\partial Q}{\partial V_{gs2}} \tag{15}$$

$$\frac{\partial C_n}{\partial V_{gs1}} = \frac{C_{ox}\left(\frac{2}{n\pi}[1-(-1)^n]k_n^2\right)}{k_n^2\left[e^{k_n t_{sc}}(C_{ox}+\varepsilon_{si}k_n)+(C_{ox}-\varepsilon_{si}k_n)\right]} = \frac{C_{ox}\left(\frac{2}{n\pi}[1-(-1)^n]\right)}{\left[e^{k_n t_{sc}}(C_{ox}+\varepsilon_{si}k_n)+(C_{ox}-\varepsilon_{si}k_n)\right]}$$

$$\frac{\partial V_{gs1}}{\partial Q} = \frac{1}{C_{ox} + \sum_{n=1}^{\infty} \frac{\partial C_n}{\partial V_{gs1}}\left(1+e^{k_n t_{sc}}\right)\left(\frac{1}{n\pi}\right)\left[(-1)^n - 1\right]}$$

$$\frac{\partial Q}{\partial V_{gs2}} = \frac{1}{2\alpha t_f + 12\beta t_f Q^2 + 30\gamma t_f Q^4 + \frac{\partial V_{gs1}}{\partial Q}}$$

Substituting Eq. (15) into Eq. (14),

$$\begin{aligned}\frac{\partial A_n(t_{SC}/2)}{\partial V_{gs2}} &= 2e^{k_n t_{sc}/2} \frac{\partial C_n}{\partial V_{gs2}} = 2e^{k_n t_{sc}/2} \frac{\partial C_n}{\partial V_{gs1}} \frac{\partial V_{gs1}}{\partial Q} \frac{\partial Q}{\partial V_{gs2}} \\ &= \frac{2e^{k_n t_{sc}/2} C_{ox}\left(\frac{2}{n\pi}[1-(-1)^n]\right)}{\left[e^{k_n t_{sc}}(C_{ox}+\varepsilon_{si}k_n)+(C_{ox}-\varepsilon_{si}k_n)\right]} \frac{1}{C_{ox}\left\{1+\sum_{n=1}^{\infty}\frac{\partial C_n}{\partial V_{gs1}}\left(1+e^{k_n t_{sc}}\right)\left(\frac{1}{n\pi}\right)\left[(-1)^n-1\right]\right\}} \times \\ &\quad \frac{1}{2\alpha t_f + 12\beta t_f Q^2 + 30\gamma t_f Q^4 + \frac{\partial V_{gs1}}{\partial Q}}.\end{aligned}$$

The SS obtained using the presented model is compared with the SS obtained from the I-V curve using 2D potential. In this case, $x_{min}=L_g/2$ was used. The SSs derived from the I-V curve, this analytical model, and TCAD with the thickness of ferroelectric material, t_f as a

parameter are compared under the conditions indicated inside Fig. 5. The dots denote SSs of TCAD in the case of t_f=0 nm in Fig. 5 [38]. Based on Fig. 5, the results are in good agreement.

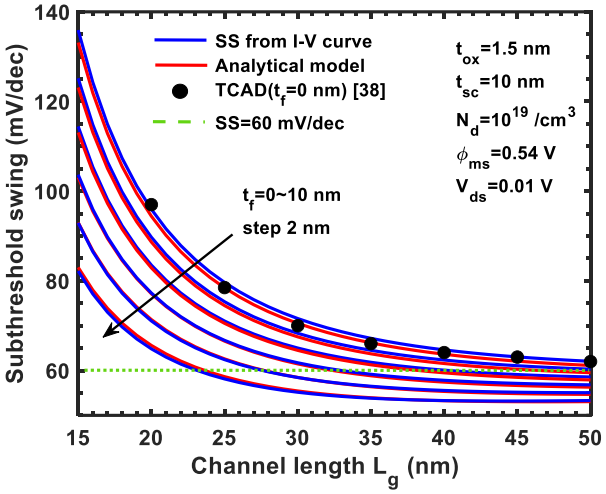

Fig. 5: Comparisons on SSs derived from I-V curve and this analytical model and TCAD [38].

Also, the analytical SS model in this paper shows good agreement with the TCAD result at t_f=0 nm, meaning it is valid. As mentioned in Figs. 2 and 3, as the thickness of the ferroelectric material increases, the SS decreases. In particular, when t_f = 10 nm under the conditions indicated inside Fig. 5, the SS values of 60 mv/dec or less were obtained even when the channel length was 28 nm. It was also observed that the size of the JLDG FET capable of observing SS of 60 mV/dec or less and the thickness of the ferroelectric material were correlated. Therefore, using the analytical SS model presented in this paper, we will analyze the SS with parameters such as the ferroelectric thickness t_f and channel length L_g. Table 1 summarizes the device parameters used in this paper.

Table 1: Device parameters for this analytical SS model

Device parameter	Symbol	Value
Channel length	L_g	15-50 nm
Channel width	W	1 μm
Channel thickness	t_{sc}	1-10 nm
SiO_2 thickness	t_{ox}	1-4 nm
Doping concentration	N_d	10^{19} /cm^3
Ferroelectric thickness	t_f	0-10 nm
Remanent polarization	P_r	17 μC/cm^2
Coercive field	E_c	1.2 MV/cm

3. ANALYSIS FOR SS OF JLDG FET WITH FERROELECTRIC

In order to observe the change of the SS with the change of the thickness of the ferroelectric material and channel length, Fig. 6 shows the change of the SS with respect to the ferroelectric thickness with the channel length as a parameter. It was observed that the SS decreased as the channel length and ferroelectric thickness increased. In particular, it can be seen that the region of SS < 60 mV/dec exists when the ferroelectric thickness, t_f is 10 nm or

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more and the channel length is 25 nm or more under conditions indicated in Fig. 6. It was also observed that the change in SS according to the channel length appeared smaller as the ferroelectric thickness increased. However, when the channel length was decreased, the SS showed a large value even though the change of SS according to the ferroelectric thickness was severe. When the channel length was increased to 50 nm, a region with SS<60 mV/dec appeared even when the ferroelectric thickness was about 1 nm. As such, ferroelectric thickness and channel length had a mutual effect on SS.

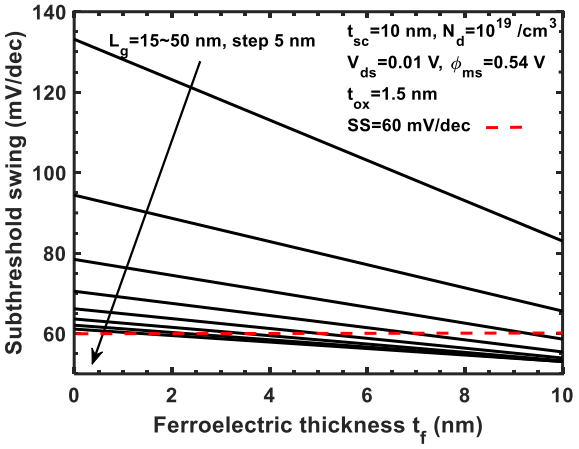

Fig. 6: The SSs for ferroelectric thickness t_f with the channel length L_g as a parameter.

The SS will vary not only with the ferroelectric thickness t_f and channel length L_g, but also with the thickness of SiO_2, t_{ox}. Figure 7 shows the contour line of SS=60 mV/dec for ferroelectric thickness and channel length with the thickness of SiO_2 as a parameter. The SS<60 mV/dec region is above the line. As can be seen in Fig. 7, the SS<60 mV/dec region changed significantly according to t_{ox}, and the SS<60 mV/dec region was observed in a wider area in the given simulation range as t_{ox} decreased. In particular, the SS=60 mV/dec line showed an inverse relationship between channel length and ferroelectric thickness. That is, if the channel length decreases, SS=60 mV/dec can be observed only when the ferroelectric thickness is increased. Figure 5 shows how ferroelectric thickness can be increased in order to decrease SS when decreasing the channel length.

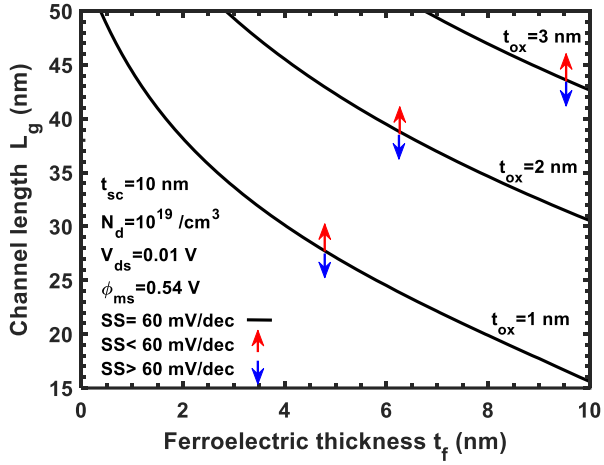

Fig. 7: Contours of SS=60 mV/dec with the thickness of SiO_2, t_{ox} as a parameter.

The SS also shows a large change according to the thickness of the silicon channel, t_{sc}. In Fig. 8, the contour of SS=60 mV/dec was plotted for channel length and ferroelectric thickness with silicon thickness t_{sc} as a parameter. In Fig. 8, it can be observed that the SS<60 mV/dec region (above the line as shown in Fig. 7) increases as silicon thickness t_{sc} decreases. Observing Fig. 8, if t_{sc}=5 nm, it can be seen that SS<60 mV/dec region exists when the ferroelectric thickness is 9 nm or more, even if the channel length is decreased to 15 nm. However, if t_{sc} =10 nm, it can be seen that SS > 60 mV/dec when the ferroelectric thickness is 2 nm or less even if the channel length is increased to 50 nm. As such, it was observed that the SS significantly decreased due to the presence of the ferroelectric material.

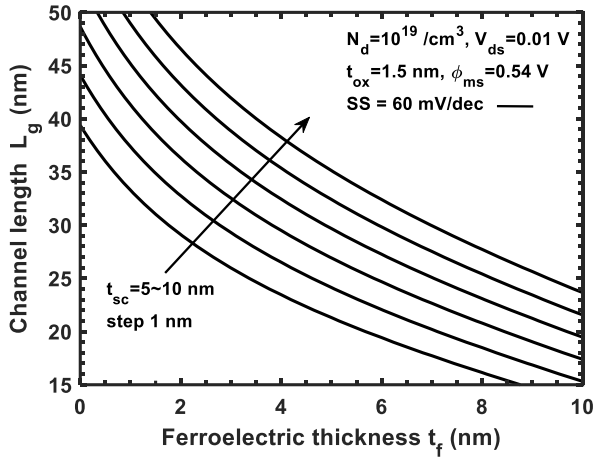

Fig. 8: Contours of SS=60 mV/dec with the thickness of silicon, t_{sc} as a parameter.

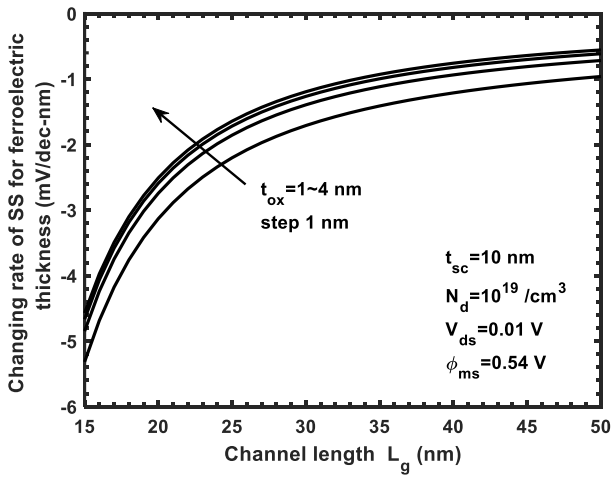

Fig. 9: Changing rate of SS for ferroelectric thickness with the thickness of SiO_2, t_{ox} as a parameter.

In order to examine the change in the SS according to the ferroelectric thickness t_f in more detail, Fig. 9 shows the change in SS ($\Delta SS/\Delta t_f$) with respect to the change in ferroelectric thickness according to the channel length with t_{ox} as a parameter. Fig. 9 illustrates how the change in SS varies with ferroelectric thickness very strongly when the channel length is as small as 15 nm. However, it was observed that the SS change with respect to the ferroelectric thickness became saturated and constant as the channel length increased. It can be seen that the change in ferroelectric thickness no longer has a significant effect on the change in SS when the channel length is increased. In other words, it can be seen that the negative capacitance effect caused by ferroelectric becomes larger as the

channel length decreases. In addition, the change of the SS with respect to ferroelectric thickness was large as the t_{ox} decreased, and it was observed that the rate of change of SS with respect to ferroelectric thickness became almost constant when the t_{ox} increased and became more than 4 nm under the conditions indicated inside Fig. 9.

The change of the SS according to the ferroelectric thickness is shown in Fig. 10 with silicon thickness t_{sc} as a parameter. As can be seen from Fig. 10, the change of the SS according to the ferroelectric thickness does not change significantly with t_{sc} when the channel length increases, but it can be seen that it changes significantly with the t_{sc} when the channel length decreases. Also, the change rate of the SS according to the ferroelectric thickness was decreasing with the channel length when t_{sc} decreased, and if t_{sc} increased to 10 nm, it was found that the change rate of SS according to the ferroelectric thickness increased significantly with the channel length. From the results of Figs. 9 and 10, it was observed that the change rate of the SS according to the ferroelectric thickness decreased with the channel length as t_{ox} was larger and t_{sc} was smaller.

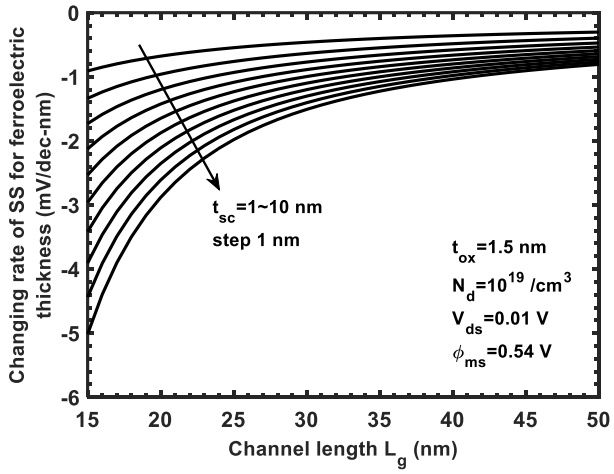

Fig. 10: Changing rate of SS for ferroelectric thickness t_f with silicon thickness t_{sc} as a parameter.

4. CONCLUSIONS

The analytical model of the SS for a JLDG FET using a gate oxide by stacking a ferroelectric material on SiO_2 is presented. If a ferroelectric material is used, a negative capacitance effect occurs due to the gate voltage amplification phenomenon, so that the SS can obtain a value of 60 mV/dec or less. The analytical SS model presented was in good agreement with the SS derived from the I-V curve obtained by 2D potential distribution. As a result of analysis using the analytical SS model, SS < 60 mV/dec was obtained when the ferroelectric thickness was 6 nm or more at a channel length of 25 nm, a silicon thickness of 10 nm, and a t_{ox} of 1 nm. In addition, the change rate of the SS according to the ferroelectric thickness was almost constant according to the channel length when the t_{sc} decreased to about 1 nm and the change of the SS according to the ferroelectric thickness was not affected by the thickness of SiO_2 when the t_{ox} increased to 4 nm or more. As can be seen from the above results, for the JLDG FET using ferroelectric, SS<60 mV/dec could be manufactured by adjusting the channel length, silicon thickness, thickness of SiO_2, and ferroelectric thickness. The analytical SS model presented in this paper can be used to analyze this phenomenon.

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