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EFFECT OF FERRO ELECTRIC THICKNESS ON NEGATIVE CAPACITANCE FET (NCFET)

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ABSTRACT: Conventional Field Effect Transistor (FET) are well known to require at least 60mV/decade at 300K change in the channel potential to change the current by a factor of 10. Due to this, 60mV/decade becomes the bottleneck of this day transistor. A comprehensive study of the Negative Capacitance Field Effect Transistor (NCFETis presented. This paper shows the effect of ferroelectric material in MOSFET structure by replacing the insulator in the conventional MOSFET. It should be possible to obtain a steeper subthreshold swing (SS) compared to the one without a ferroelectric material layer, thus breaking the fundamental limit on the operating voltage of MOSFET. 27% of the subthreshold slope reduction is observed by introducing ferroelectric in the dielectric layer compared to the conventional MOSFETs. Hence, the power dissipation in MOSFET can be mitigated and shine to a new technology of a low voltage/low power transistor operation.

ABSTRAK: Transistor Kesan Medan Konvensional (FET) terkenal memerlukan sekurang-kurangnya 60mV / dekad pada 300K perubahan pada saluran yang berpotensi untuk mengubah arus dengan faktor 10. Oleh kerana itu, 60mV / dekad menjadi hambatan transistor hari ini. Kajian komprehensif mengenai Negative Capacitance Field Effect Transistor (NCFETis dikemukakan. Makalah ini menunjukkan kesan bahan ferroelektrik dalam struktur MOSFET dengan mengganti penebat dalam MOSFET konvensional. Sebaiknya dapatkan swing swing subthreshold (SS) yang lebih curam berbanding dengan satu tanpa lapisan bahan ferroelektrik, sehingga melanggar had asas pada voltan operasi MOSFET. 27% pengurangan cerun subthreshold diperhatikan dengan memperkenalkan ferroelektrik di lapisan dielektrik berbanding dengan MOSFET konvensional. Oleh itu, pelesapan daya dalam MOSFET dapat dikurangkan dan bersinar dengan teknologi baru operasi transistor voltan rendah / kuasa rendah.

KEYWORDS: *NCFETs, Ferroelectric, Subthreshold*

1. INTRODUCTION

Moore's Law drove the scaling trend of Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET). Moore's idea was that the transistor's size would double every 18 months, making the transistor consume less power, become smaller in size, and perform at high speed [1]. Though the downscaling of MOSFET for the past decades continues to grow, it causes another problem to arise, such as short-channel effect, higher power consumption, and gate oxide tunneling effect [2].

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However, researchers have come out with many possible solutions to make sure Moore's Law can be held for the long run. Feedback FET [3], Tunnel FET [4], and Impact- ionization MOSFET [5] are some technologies introduced to hold MOS scaling limits. Yet, Moore's Law is almost reaching its fundamental limit [6]. Therefore, new technologies and physic are needed to cope with the MOS scaling. The voltage scaling of the supply voltage (V_{DD}) almost stopped as a further reduction of the device size, and hence the threshold voltage (V_{TH}) causes the exponential increase in the OFF state current (I_{OFF}). This is a direct consequence of the non-scalability of the subthreshold swing (SS) to below 60 mV/decade. The negative capacitance FET (NCFET) has been proposed by Salahuddin et al. [7-8] as an alternative steep slope transistor to overcome the classical limit of 60mV/dec, and has been extensively studied [8-16].

In this paper, the effect of ferroelectric thickness and doping concertation in NCFETS is analyzed to observe the device's performance, which may give further insight for future device consideration.

2. DEVICE STRUCTURE

The NCFET is designed considering 20nm gate length. Figure 1 and Table 1shows the device structure and its parameters, respectively.

The S/D depths were designed to be shallow (10nm) is to avoid punch-through occurs which typically occurs at lower voltage with a deeper source-drain junction depth. Silicon doped hafnium oxide (Si: HfO2) was used as a ferroelectric material layer due to its superior performance, such as nonvolatility, hysteresis-free, and compatible with complementary metal-oxide-semiconductor transistor (CMOS) technology [17]. A buffer layer is used to reduce the gate leakage current and improve the electrical properties of the NCFET [17].

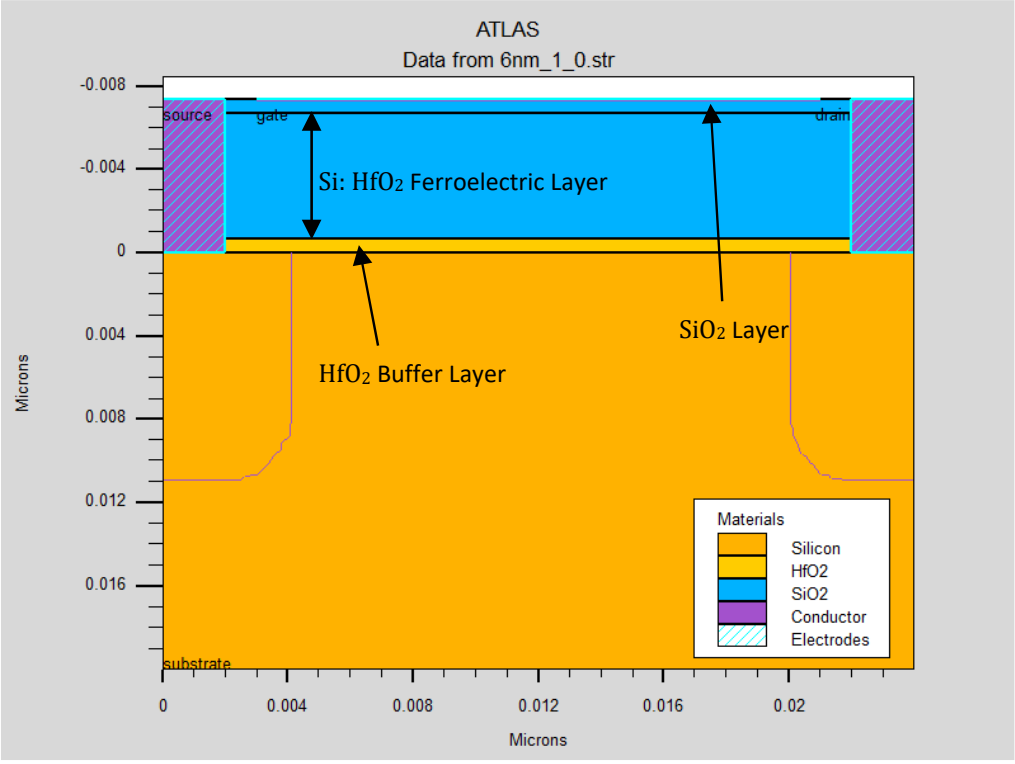

Figure 1: NCFET structure (dimension in microns)

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Table 1: Parameters used for the simulation

Parameter	Value
P-well Doping (cm^{-3})	1×10^{15}
Source/Drain Doping (cm^{-3})	1×10^{20}
Junction depth (nm)	10
Gate Metal Length (nm)	20
HfO_2 Buffer Layer Thickness (Å)	7
Ferroelectric Layer	Si: HfO_2

In this paper, five different ferroelectric material layers were used as mentioned in Table 2, various parameters for the thickness are shown. Pseudocode is developed to calculate the parameters of any given thickness of ferroelectric material based on Miller [18].

Table 2: Ferroelectric material parameters for different thickness

Ferroelectric Thickness (nm)	Remanent polarization, P_r (μC/cm²)	spontaneous polarization, P_s (μC/cm²)	E_C (MV/cm)	ε_f
2	11.8	12.50	1.18	34.8
4	11.1	11.75	1.16	34.1
6	10.4	11.00	1.14	33.4
8	9.7	10.25	1.12	32.7
10	9.0	9.50	1.10	32.0

As the ferroelectric material's thickness increases, the parameters related to the ferroelectric material; remanent polarization, spontaneous polarization, critical electric field, and zero-field relative permittivity decreased. As a result, it can be concluded that the ferroelectric properties are inversely proportional to ferroelectric thickness. This information will help us determine the ferroelectric material parameters when designing a gate structure of MOSFET with the ferroelectric material.

3. RESULTS AND DISCUSSION

The performance of the NCFETs is observed for different thickness of the ferroelectric thickness, the source-drain doping concentration in I-V characteristics, and subthreshold behavior of the MOSFETs.

3.1 Effect of Ferroelectric Layer Thickness on I-V Characteristics ions

Five transistors with different ferroelectric material layer thickness, as mentioned in Table 2, were created using the simulator. All these devices have a buffer layer of 7 Å of HfO2. The simulation on the devices with different ferroelectric material layers is carried out by using Silvaco TCAD to investigate the effect of thickness of the ferroelectric material layer on the I-V characteristics of the devices with 0.5V, 1.0V, and 1.5V gate voltages. Figure 2 shows the I-V characteristics of the devices for various ferroelectric thicknesses.

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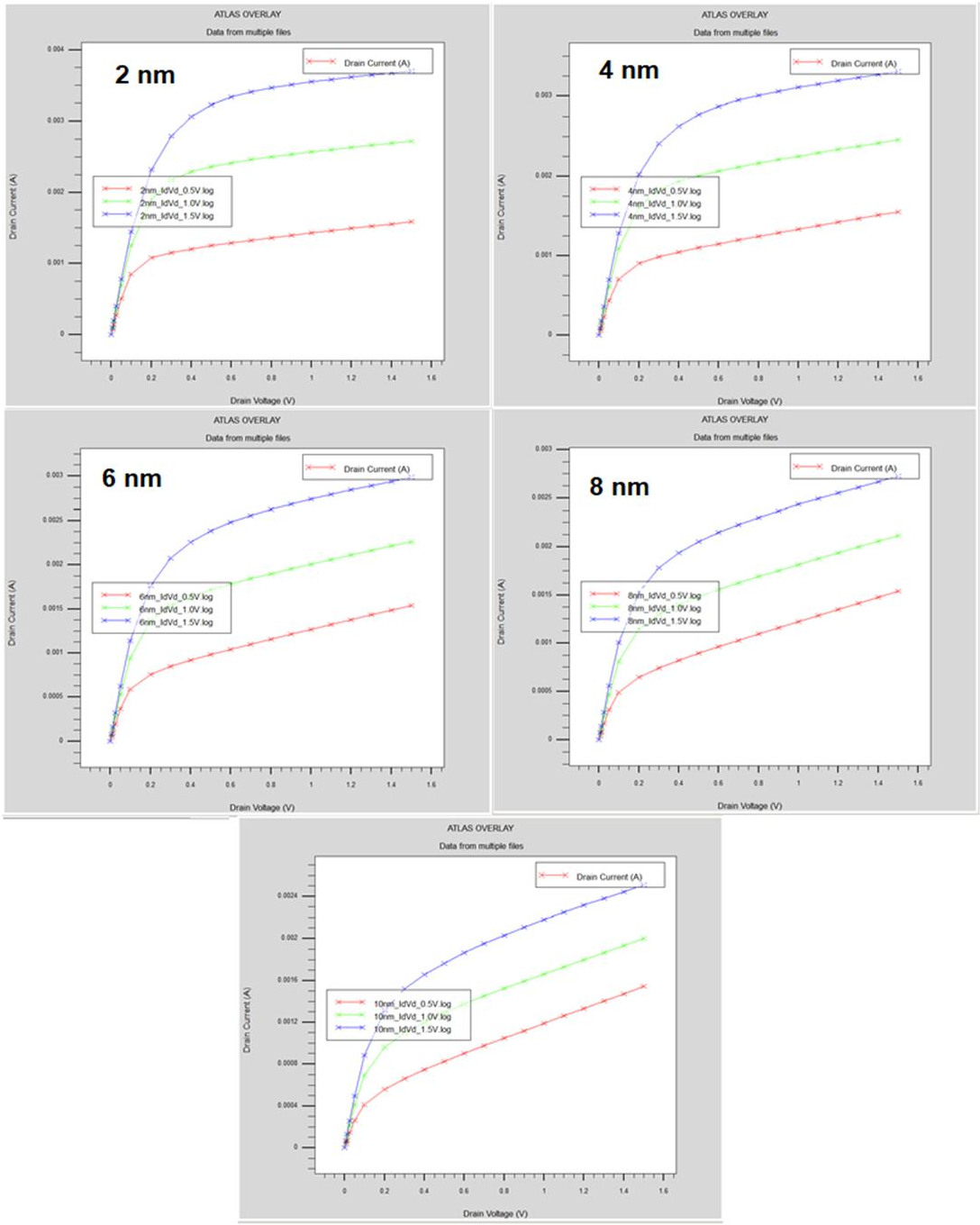

Fig. 2. I-V Characteristics of the NCFET for 2 nm to 10 nm ferroelectric layer.

The simulation shows that the saturation slope is decreasing while the current density was increasing. As the thickness increases, the variation of the slope of the drain current increases, and instead of saturation current the behavior of the transistors are moral-less resistive.

Figure 3 shows the variation of maximum drain current at V_{DS} = 1.5 V for different gate voltages and the slope at saturation with the ferroelectric thickness variation. It is observed that there is not much increment in drain current for 10nm, 8nm, and 6nm. But as the thickness of ferroelectric material decreased, in this case, 4nm and 2nm, the drain current also increased considerably. For example, for 10nm, 8nm, and 6nm cases, when the gate voltage is bias with 0.5V, there is not much increment. Figure 2 shows that as the thickness of ferroelectric material

decreased, the current increase from 1.55mA to 1.59mA for a 0.5V gate bias voltage. The same case can be seen when the gate bias voltages are 1.0V and 1.5V, the drain current increase from 2.46mA to 2.73mA and from 3.31mA to 3.7mA, respectively. It can be concluded that the thickness of ferroelectric material plays a vital role in the performance of the NCFET.

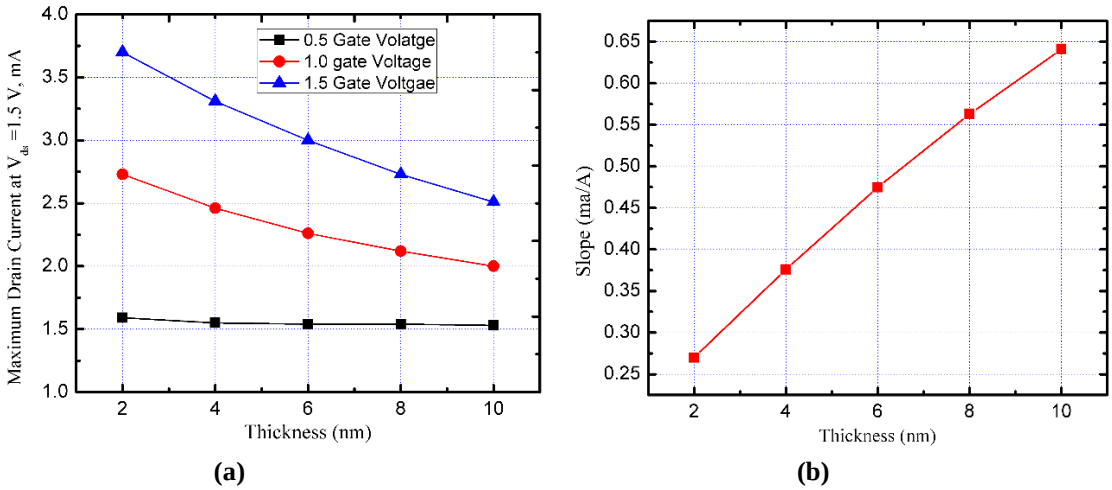

Fig. 3 (a) Variation of the maximum drain current at VDS = 1.5 V for different gate voltages and (b) slope at saturation with the variation of the ferroelectric thickness.

3.2 Effect Of Source Drain Doping Concentration To The I-V

For this simulation, 2nm ferroelectric material thickness is chosen as it gives a higher drain current at lower drain voltage, and source and drain concentration are varying, and the effect of doping concentration on the I-V characteristics are observed and shown in Fig. 4.

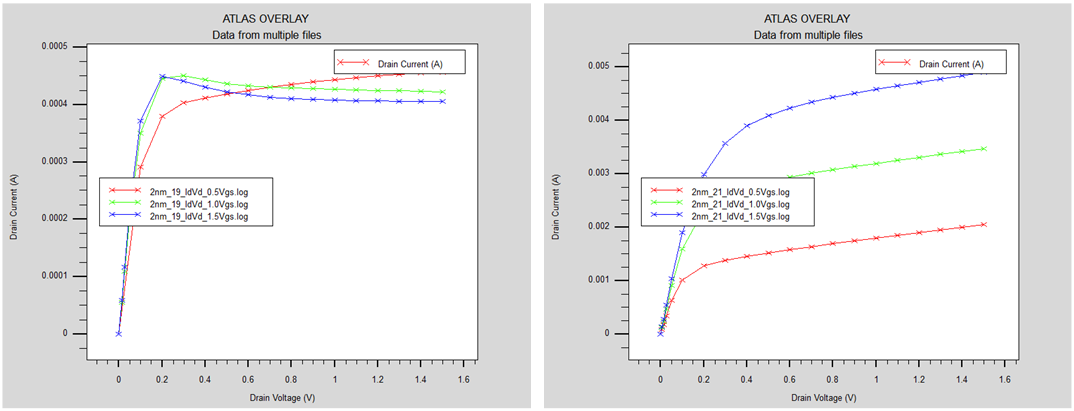

Fig. 4. I-V characteristics of 2nm ferroelectric layer NCFET for 1 x 10^{19}cm^{-3} and 1 x 10^{21}cm^{-3} source drain doping concentration respectively.

It is observed that the doping concentration of source-drain increased, the drain current density also increased. However, when the concentration is at 1 x 10^{19} cm^{-3}, there is a high current density observed for 0.5V and 1.0V gate bias voltage, but at a certain point, the current drop and become constant afterward. This effect is said to be a short channel effect due to the results of two-dimensional potential distribution and high electric fields in the channel region. For a given channel doping concentration, as the channel's length is reduced, the depletion layer width of source and drain becomes equal or comparable to the channel length. Failing current

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saturation due to the punch-through effect [19]. These results show that the doping concentration of source-drain plays a vital role in the performance of the NCFET.

3.3 Subthreshold Slope Behavior

For a Field-Effect transistor, the minimum voltage swing needed to turn a transistor from on to off is an important parameter that can be used to define the power dissipated by the device. Drain current with the variation of gate voltage (Id versus Vg) are shown in Fig. 5 for the V_{DS} of 0.05 V, 0.5 V, and 1.0 V, respectively, with different views by scaling up.

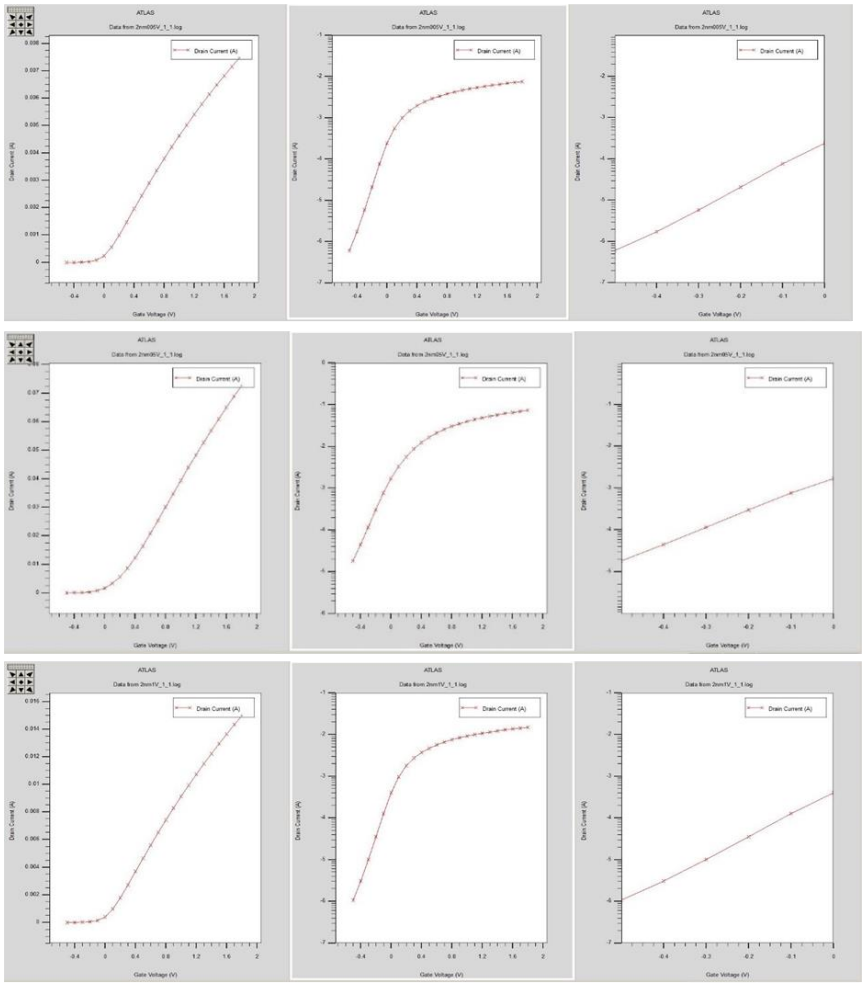

Fig. 5. I_{DS} *versus* V_{GS} for V_{DS} 0.05 V,0.5 V, and 1.0 V.

Table 3. Result for different drain bias voltage and subthreshold slope

Drain Bias Voltage (V)	Subthreshold Slope (mV/dec)
0.05	270.323
0.5	348.37
1.0	481.67

The results are tabulated in Table 3, and it is observed that with a lower drain bias voltage, the subthreshold also decrease. This means NCFET can give a steeper subthreshold slope at a lower drain bias voltage.

The input characteristics of the NCFETs and MOSFETs are shown in Fig. 5 in linear and logarithm scale. The NCFETs gives a larger drain current compared to MOSFETs. The NCFET and MOSFET subthreshold slope are 348.37 mV/dec and 446.45 mV/dec for the same device dimensions. The subthreshold slope for the one without ferroelectric material is much higher than the one with the ferroelectric material layer. This shows that, by introducing the ferroelectric material layer to the structure of MOSFET, it is possible to get a steeper subthreshold swing, thus improving the device's performance.

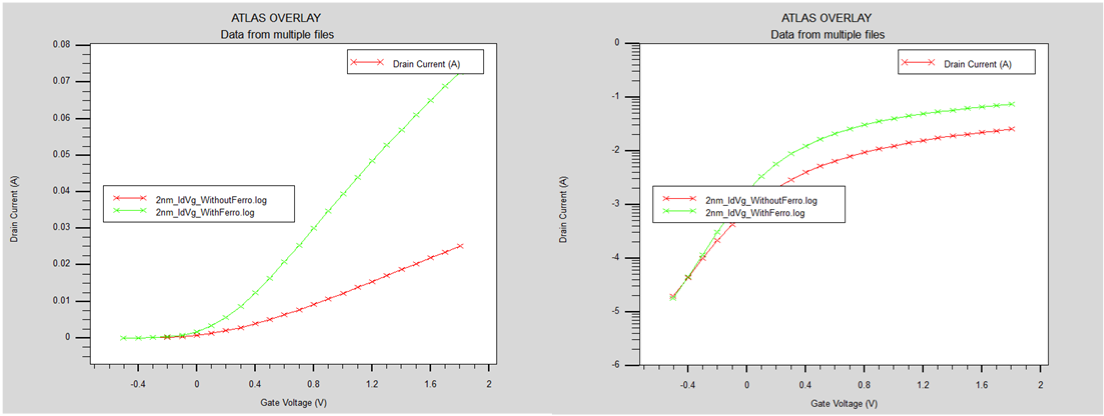

Fig. 5. I_D - V_{GS} graph the structure with ferroelectric material and without a ferroelectric layer.

4. CONCLUSION

In conclusion, a steeper subthreshold slope for NCFET compared to conventional MOSFET has been demonstrated. It is also shown that the performance of NCFET is affected by the thickness of ferroelectric material and source/drain concentration doping. As the thickness of the ferroelectric material layer decreased, a steeper I_D - V_{DS} is observed. While as the source/drain concentration doping increased, a steeper I_D - V_{DS} graph is noticed. It is remarkable that by manipulating the ferroelectric material's thickness and the source/drain doping concentration, the transistor performance can be improved for the NCFET.

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REFERENCES

[1] G. M. Moore (1965) Moore's Law, Electronics. Electronics 38(8): 114. [Online].Available:https://newsroom.intel.com/wpcontent/uploads/sites/11/2018/05/moores-law-electronics.pdf.

[2] S. Chopra and S. Subramaniam (2015) A Review on Challenges for MOSFET Scaling. Int. J. Innov. Sci. Eng. Technol. 2(4): 1055–1057. [Online]. Available: http://ijiset.com/vol2/v2s4/IJISET_V2_I4_169.pdf

[3] C. W. Yeung (2014) Steep On / Off Transistors for Future Low Power Electronics. Online http://www2.eecs.berkeley.edu/Pubs/TechRpts/2014/EECS-2014-226.pdf
[4] U. E. Avci, R. Rios, K. J. Kuhn, and I. A. Young (2011) Comparison of power and performance for the TFET and MOSFET and considerations for P-TFET. Proc. IEEE Conf. Nanotechnol. pp. 869–872. https://doi.org/10.1109/NANO.2011.6144631
[5] K. E. Moselund, D. Bouvet, V. Pott, C. Meinen, M. Kayal, and A. M. Ionescu (2008) Punch-through impact ionization MOSFET (PIMOS): From device principle to applications. Solid. State. Electron. 52(2): 1336–1344. https://doi.org/10.1016/j.sse.2008.04.021
[6] M. Kobayashi , Kyokai Joho Imeji Zasshi (2016) More than moore. Journal Inst. Image Inf. Telev. Eng. 70(3): 324–327. https://doi.org/10.3169/itej.70.324
[7] S. Salahuddin and S. Datta (2008) Can the subthreshold swing in a classical FET be lowered below 60 mV/decade?" Tech. Dig. Int. Electron Devices Meeting. pp. 693–696. https://doi.org/10.1109/IEDM.2008.4796789
[8] S. Salahuddin and S. Datta (2008) Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices. Nano Lett., 8 (2): 405–410. https://doi.org/10.1021/nl071804g
[9] X. Li, J. Sampson, A. Khan, K. Ma, S. George, A. Aziz et al. (2018) Enabling Energy-Efficient Nonvolatile Computing With Negative Capacitance FET. IEEE Transactions on Electron Devices. 64(8): 3452-3458. https://doi.org/10.1109/TED.2017.2716338
[10] S. C. Chang, U. E. Avci, D. E. Nikonov and I. A. Young (2017) A Thermodynamic Perspective of Negative-Capacitance Field-Effect Transistors. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits. 3(1): 56-64. https://doi.org/10.1109/JXCDC.2017.2750108
[11] Ko E, Shin J, Shin C (2018) Steep switching devices for low power applications: negative differential capacitance/resistance field effect transistors. Nano Convergence.5(1):2. https://doi.org/10.1186/s40580-018-0135-4
[12] A. Sharma and K. Roy (2017) Design Space Exploration of Hysteresis-Free HfZrOx-Based Negative Capacitance FETs. IEEE Electron Device Letters.38(8):1165-1167. https://doi.org/10.1109/LED.2017.2714659
[13] A. I. Khan, K. Chatterjee, B. Wang, S. Drapcho, L. You, C. Serrao, S. R. Bakaul, R. Ramesh, and S. Salahuddin (2015) Negative capacitance in a ferroelectric capacitor. Nature Materials. 14(2): 182-186. https://doi.org/10.1038/nmat4148
[14] Saptarshi Das (2016) Two Dimensional Electrostrictive Field Effect Transistor (2D-EFET): A sub-60mV/decade Steep Slope Device with High ON current. Scientific Reports. 6: 34811. https://doi.org/10.1038/srep34811
[15] S. H. Le, B. R. Salmassi, J. N. Burghartz,, P. M. Sarr (2004) Characterization of ferroelectric thin films materials for FeRAM. Proc SAFE & Prorisc Veldhoven, pp. 710-713.
[16] Fei Liu, Yan Zhou, Yijiao Wang, Xiaoyan Liu, Jian Wang and Hong Guo (2016) Negative capacitance transistors with monolayer black phosphorus. npj Quantum Materials. 2016: 16004: 1-6. http://dx.doi.org/10.1038/npjquantmats.2016.4
[17] L. Tu, X. Wang, J. Wang, X. Meng, and J. Chu (2018) Ferroelectric Negative Capacitance Field Effect Transistor," Adv. Electron. Mater. 4(11):1–17. https://doi.org/10.1002/aelm.201800231
[18] S. L. Miller and P. J. McWhorter (1992) Physics of the ferroelectric nonvolatile memory field effect transistor. J. Appl. Phys.72(12):5999–6010. https://doi.org/10.1063/1.351910
[19] Faculty of NPTEL, "Module 2?: MOSFET Lecture 8?: Short Channel Effects," p. 6, [Online]. Available: http://nptel.ac.in/courses/117101058/downloads/Lec-8.pdf.